DESIGN OF A FIRST-ORDER DELTA-SIGMA OVERSAMPLING MODULATOR WITH NOISE CONSTRAINTS

BY

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ABSTRACT

In this thesis, a low noise, first-order, delta-sigma analog to digital modulator (ΣΔM) has been designed using a standard 0.5um CMOS process. The modulator is an amalgam of several other circuits including a folded-cascode transconductance amplifier, a latched comparator, a switched capacitor filter and a digital to analog converter (D/A). In each case, Tanner Tools™ software was used to generate the circuit schematic and layout. In addition, the Tanner™ package was used for the simulation and verification of all circuits. The ΣΔM was created using an approach that greatly speeds up the design, layout and verification process. Instead of using a conventional layout approach that requires each transistor to be individually designed, pre-drawn transistor pairs were implemented and wired to form the completed circuit. This approach allows complex circuits to be realized quickly. In addition, since all transistors used in the circuit layout originate from one or two transistor pairs, this approach greatly simplifies the verification process.

Prior to the design of the ΣΔM, the Tanner Tools™ suite was updated from a 1.6um technology to a newer and smaller 0.5um minimum feature size. This report details much of the work that was required to complete the transition from the old process to the new process. Moreover, several parts of the ΣΔM were scaled from the 1.6um minimum feature size to the newer, 0.5um technology. Two chips are currently being fabricated by the MOSIS service using 0.5um technology. The first design contains several individually wired parts of the ΣΔM. This chip will allow each part of the ΣΔM to be tested individually in the event to the ΣΔM does not perform as expected. The second design contains a complete ΣΔM that is wired on-chip. This design will allow the ΣΔM to be tested as a whole to verify its correct operation.

This report will show through simulation that in most cases, the newer 0.5um designs were able to achieve higher gain and switch more quickly. Each circuit was simulated using 1.6um and 0.5um process parameters that were supplied by the MOSIS service. Furthermore, the simulations will show the operating potential of the completed ΣΔM.

1. INTRODUCTION

The development of effective, low noise analog-to-digital converters has become necessary due to the rapid progression of digital electronics. While digital signals and devices are universally recognized as cutting-edge technologies, many electronics still utilize analog technology.

The purpose of this study is to design a low noise, first-order delta-sigma analog to digital converter which is also known as delta-sigma modulator (ΔΣM). At the core of the ΔΣM, a switched capacitor circuit functions as a low pass filter while the actual signal quantization is performed in combination with a latched comparator. Switched capacitor filters have proven to be an effective alternative to traditional RLC filters due to their small size and ease of integration. In contrast, filters that utilize passive components are generally large and take up a great deal of space on a chip.

Fundamentally, a latched comparator consists of a high-speed operational amplifier (op-amp) with some additional circuitry (latch) to control the amplifier slew rate. The addition of the latch effectively limits the output of the comparator and allows the comparator output to quickly slew in the opposite direction.

The proposed design will be created using an AMI 0.5 micron process. Consequently, existing designs that were drawn using a larger minimum feature size will be scaled to fit the new technology requirements. The use of smaller minimum feature size allows designs to use less space on a wafer and utilize more recent fabrication techniques. Tanner Tools^{TM} will be used to design, simulate and prepare the layout of the ΔΣM for subsequent fabrication. Actual prototype fabrication will be performed by the MOSIS service using an AMI 0.5um process.

1.1 The MOSFET

Metal Oxide Semiconducting Field Effect Transistors (MOSFET) are the foundation of modern CMOS technology. While many circuit designers consider the MOSFET to be a cutting-edge technology, the basic idea on which the MOS transistor is based is over a half century old.[3] A 3-input, n-channel MOS transistor is shown in Figure 1.1.

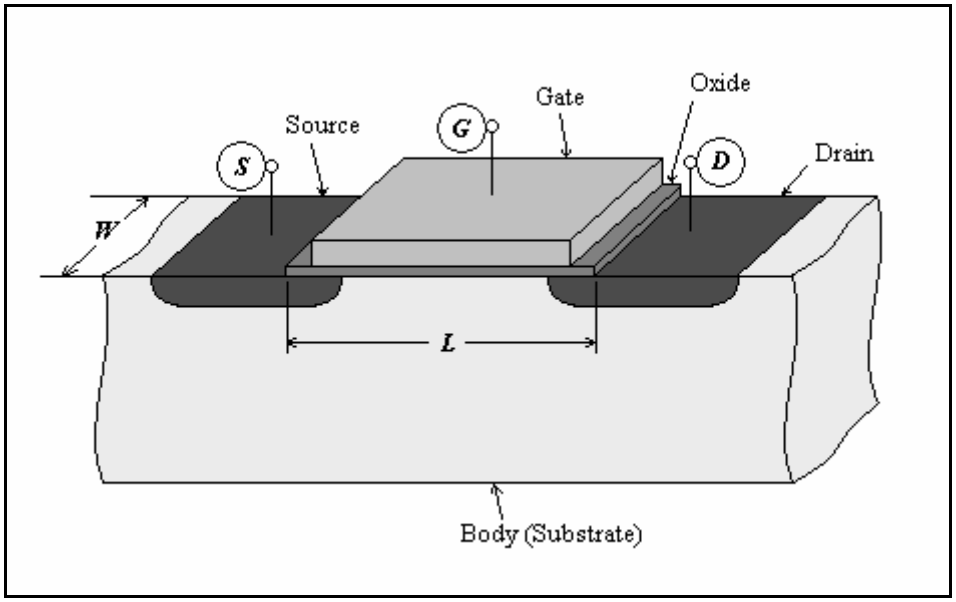

Figure 1.1: Structure of an n-channel MOSFET

As illustrated in Figure 1.1, the bulk of the n-channel MOSFET is formed on a p-type silicon wafer known as the body. Both the source and drain of the n-channel MOSFET are formed on the wafer and are doped n-type. The center of the transistor is covered by a thin, insulating oxide layer such as silicon dioxide. The gate of the transistor is completed by depositing a layer of polycrystalline silicon on top of the gate-oxide layer.

The region between the source and drain is known as the channel. The width/length of the channel is referred to as the transistor aspect ratio and will vary depending on the circuit design needs.

When the gate of an n-channel MOSFET is made sufficiently positive, electrons from the body (or bulk) will be attracted directly below the insulating oxide. Consequently, an n-type channel will form and current will be allowed to flow directly from the source to the drain. The transistor threshold voltage (V_{tn}), is the gate source-voltage (V_{GS}) where the concentration of electrons under the gate is equal to the concentration of holes in the substrate[7]. When the gate-source voltage is smaller than the threshold voltage ($V_{GS} < V_{tn}$), the channel is not present and current will not flow between the source and drain. As the gate-source voltage is increased to V_{tn}, eventually the required number of electrons will accumulate under the gate and form a channel between the source and drain. If V_{GS} is increased beyond V_{tn}, the density of electrons within the channel will increase.[7] This logic demonstrates that the gate source voltage is proportional to the density of electrons in the channel and ultimately, the charge density. The charge density is called the effective gate source voltage (V_{eff}) and can be determined using Equation 1.1.1.

$$V_{eff} = V_{GS} - V_{tn} \tag{1.1.1}$$

The charge density is given by:

$$Q_n = C_{OX}(V_{GS} - V_{tn}) = C_{OX}V_{eff} \tag{1.1.2}$$

where Q_n is the charge density, V_{GS} is the gate-source voltage, V_{tn} is the threshold voltage and V_{eff} is the effective gate source voltage when both the drain and source voltages are zero. C_{OX} is the gate capacitance per unit area and is given by:

$$C_{OX} = \frac{K_{OX}\varepsilon_0}{t_{OX}} \tag{1.1.3}$$

where K_{OX} is the relative permeability of SiO_2 and t_{OX} is the thickness of the gate oxide. It is important to note that Equation 1.1.3 is a measure of the gate capacitance per unit

area. The total gate capacitance (C_{GS}) can be expressed as the product the transistor aspect ratio (W/L) and C_{OX}.

$$C_{GS} = (WL)C_{OX} \quad \textbf{(1.1.4)}$$

Similarly, the total charge of channel ($Q_{T\text{-}n}$) is proportional to the product of the total gate capacitance and the effective gate source voltage.

$$Q_{T-n} = (WL)C_{OX}(V_{GS} - V_{tn}) = (WL)C_{OX}V_{eff} \quad \textbf{(1.1.5)}$$

Next, if a voltage (V_{DS}) is allowed to flow from the drain to the source of the transistor, the relationship between V_{DS} and the drain current (I_D) can be determined by the following Equation[7]:

$$I_D = \mu_n Q_n \frac{W}{L} V_{DS} \quad \textbf{(1.1.6)}$$

where μ_n is the approximate mobility of electrons near the surface of silicon and Q_n is the charge concentration of the channel per unit area. Substituting Equation 1.1.5 into 1.1.6 produces the following result:

$$I_D = \mu_n C_{OX} \frac{W}{L}(V_{GS} - V_{tn})V_{DS} = \mu_n C_{OX} \frac{W}{L} V_{eff} V_{DS} \quad \textbf{(1.1.7)}$$

This Equation provides a direct correlation between the effective drain-source voltage and the amount of current allowed to flow through the transistor. A circuit designer can draw several important conclusions from this model:

- The drain current is dependent on the aspect ratio of the transistor. If the width of the transistor is sufficiently larger than the transistor length, the transistor will allow more current to flow.

- The drain current is dependent on the process parameters (C_{OX}, K_{OX}, etc.). This is an important observation because as this report will later show, the simulation results will vary greatly from one process to another.

1.2 Analog to digital conversion

While digital circuit design is considered a cutting-edge technology, many analog sensors are still in production and use by the general public. Consequently, a conflict arises because devices that use digital technology are incapable of direct interaction with analog technology. Likewise, analog devices are unable to directly communicate with digital devices. As one can see, there is a need for a device that allows the two technologies to collaborate with one another.

Analog to digital conversion is the process whereby an analog or continuous signal is converted to a pulsed or discrete signal. An analog to digital converter (ΣΔM) is an electronic device which converts an analog signal to a digital output. These types of devices serve as a translator between analog and digital technologies.

This report focuses on the design of particular type of analog-to-digital converter, known as a Delta-Sigma modulator (ΔΣM). This type of converter is universally known for its ability to achieve high resolution.[1] In addition, this type of filter is sometimes referred to as a noise-shaping filter because of its ability to manipulate the circuit signal-to-noise ratio (SNR).

1.2.1 ΔΣ oversampling modulators

In this report a first-order, delta-sigma modulator (ΔΣM) is described. The proposed design utilizes a switched-capacitor filter which samples the analog voltage applied to the inputs of the circuit and then additional circuitry converts the sample to a digital output. These types of circuits, which are known as sampling or sample and hold

circuits, are commonly used in analog-to-digital and digital-to-analog conversion.[8] A basic sample and hold circuit is illustrated in Figure 1.2.

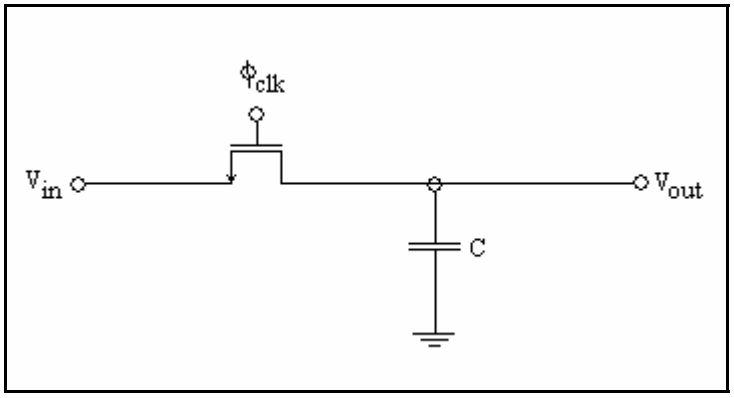

Figure 1.2: Basic Sample-and-Hold Circuit

When the signal Φ_{clk} is high, the transistor is on and the capacitor (C) is charged to V_{in}. Ideally, when Φ_{clk} is low, the transistor is off and the value of V_{in} is stored by capacitor (C). However, when thermal noise is present, the resistance when the transistor is switched on causes the capacitance voltage noise (V_{CN}) to be equal to Equation (1.2.1):[7]

$$V_{CN} = \sqrt{\frac{kT}{C}} \qquad \textbf{(1.2.1)}$$

Where C is the capacitance, k is Boltzmann's constant and T is the temperature. This Equation indicates that when the transistor is turned off, the capacitor C stores the value of V_{in} and the thermal noise voltage V_{CN}. Clearly, it can be seen that if a single sample of the input it taken, it will always be offset by the noise voltage V_{CN}.

Oversampling circuits are designed to minimize the occurrence of quantization noise by taking many samples of the input and averaging them together. If more samples are averaged, then the circuit is able to realize a more accurate measurement of the input. The number of samples taken is controlled by the circuit clock, Φ_{clk}.

This concept is easily understood by considering the operation of the circuit shown in Figure 1.3 when a DC voltage is applied. If the circuit takes one sample of the

DC voltage, then the value held will be equivalent to the sum of the DC voltage level and the RMS value of the noise voltage. However, if Φ_{clk} is increased such that the circuit takes twenty samples, then Vin increases linearly while the noise increases as V_{RMS}. Thus, the signal to noise ratio (SNR) increases. As one can see, this technique can effectively yield a more accurate measurement of the input voltage. Furthermore, it can be seen that is best to take as many samples as possible in order to achieve a highly accurate measurement.

Unfortunately, traditional modulators such as successive approximate filters A/D converters operate at speeds much lower than the circuit Nyquist rate. As the sampling rate of a traditional modulator is increased, the circuit is unable to produce meaningful output. Consequently, there is a need for modulators that operate much faster than the circuit Nyquist rate. Such devices are known as oversampling modulators. The general architecture of a first-order ΔΣM is illustrated in Figure 1.3.

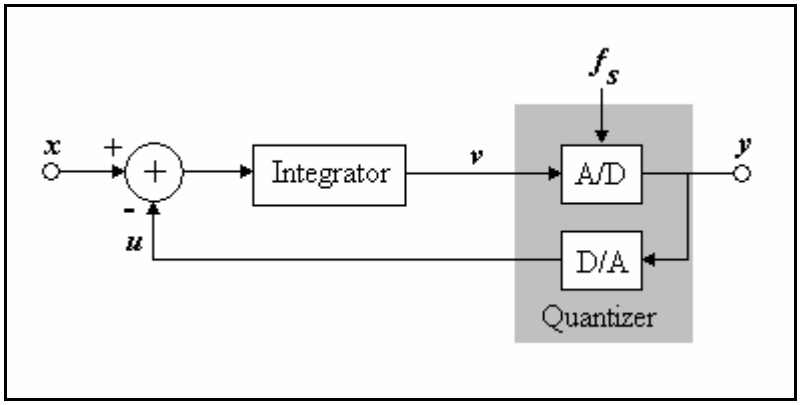

Figure 1.3: Architecture of an Oversampling Delta-Sigma Modulator

As illustrated, the modulator has two keys parts; an integrator and a quantizer. As its name suggests, the integrator effectively integrates an analog or sinusoidal input (x) and converts it to a low resolution discrete output (v). The name first-order, refers to that fact that only one integrator is present in the forward path of the modulator.

Next, the output of the integrator is processed by the quantizer at the sampling rate speed, f_s. During this stage, the low resolution output of the integrator (v) is converted to a high resolution signal (y) at a lower sampling rate.[6] In this report, the A/D is realized using a simple latched comparator.

When the input of the A/D is high (above ground), a one bit D/A feeds a positive reference signal into the inputs of the integrator that is subtracted from the input signal. Likewise, when the input of the A/D is low, the D/A feeds a negative reference signal into the integrator which is added to the input signal. The integrator accumulates the difference between the input and reference signals because the D/A only has two possible outputs that are fed into the input. The result is a linearization of the circuit's output.

1.2.2 Consequence of oversampling

The term "oversampling" describes types of analog-to-digital converters that sample much faster than the circuit Nyquist rate. The oversampling rate is defined as the ratio of the sampling rate to the Nyquist rate. This relationship is defined by Equation (2.2.2): [9]

$$OSR = \frac{f_s}{2f_o} \qquad \textbf{(1.2.2)}$$

where $2f_o$ is the Nyquist rate and f_s is the sampling rate. It will be shown that by operating at speeds much higher than the Nyquist, noise effects can be reduced.

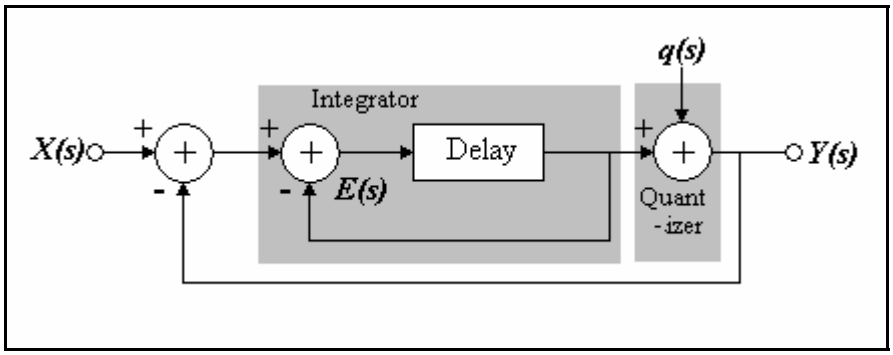

Figure 1.4: First-Order Delta-Sigma Modulator Noise Model

Figure 1.4 illustrates a noise model for a typical first-order delta-sigma modulator. During the quantization process (i.e. the signal is converted to a digital output), a certain amount of error (q) is introduced into the signal output (y). The error can be determined by calculating the difference between the modulator output (y) and the quantizer input (v). It is assumed that much of this noise is white quantization noise or in other words, noise that is constant over a given frequency. [10]

The input-output relationship of the modulator shown in Figure 1.4 can be derived using the following approach:

$$E(s) = X(s) - Y(s) \tag{1.2.3}$$

Rewriting in terms of the output produces:

$$Y = E(s)H(s) + q(s) \tag{1.2.4}$$

Substituting 1.2.3 into Equation (1.2.4) yields:

$$Y = (X(s) - Y(s))H(s) + q(s) \tag{1.2.5}$$

Solving Equation (1.2.5) in terms of Y(s) produces:

$$Y(s) = \frac{X(s)H(s) + q(s)}{1 + H(s)} \tag{1.2.6}$$

$$Y(s) = \frac{X(s)H(s)}{1 + H(s)} + \frac{q(s)}{1 + H(s)} \tag{1.2.7}$$

As seen in Equation (1.2.7), $\frac{1}{1 + H(s)}$ is the noise transfer function. If $H(s) = \frac{1}{s}$ (an integrator), than Equation (1.2.7) can be rewritten as:

$$Y(s) = \frac{\frac{1}{s}X(s)}{1+\frac{1}{s}} + \frac{q(s)}{1+\frac{1}{s}} \qquad \textbf{(1.2.8)}$$

Simplifying Equation (1.2.8) yields:

$$Y(s) = \frac{X}{s+1} + \frac{sq(s)}{s+1} \qquad \textbf{(1.2.9)}$$

In general, the delta-sigma modulator is operated at low frequencies. Consequently, a more general form of Equation 1.2.9 can be written as:

$$Y(s) = X + sq(s) \qquad \textbf{(1.2.10)}$$

Equation (1.2.10) shows that a zero is present in the noise transfer function. Consequently, the resultant noise of the modulator is high passed as illustrated in Figure 1.5. This is called "noise shaping."

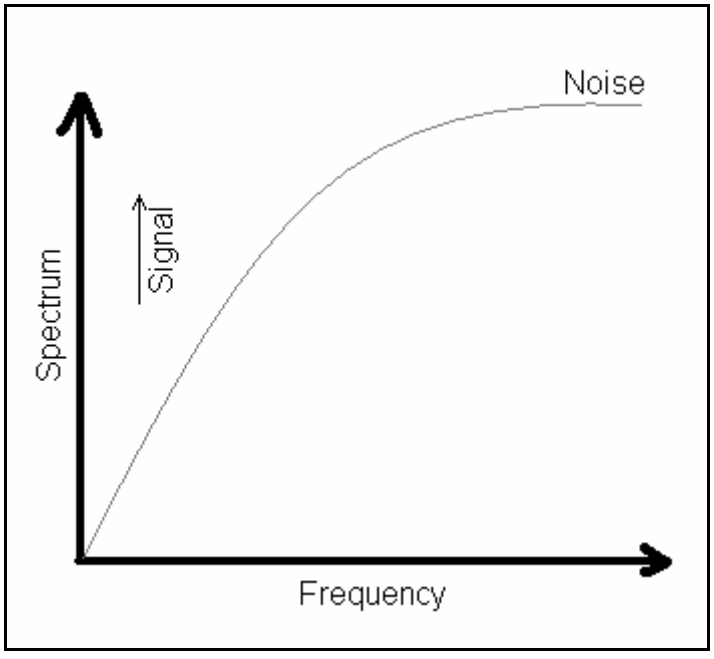

Figure 1.5: High-Passed Noise

1.3 Proposed Work and Thesis Goals

First, the circuit design tools must be upgraded from a 1.6um minimum feature size to a smaller, 0.5um process. Most of this work will focus on modifying the circuit layout tool, L-Edit™. Several of layout tools features including the Design Rule Checker (DRC), Layer Manager and Extraction files must be modified in order to accept the new minimum feature size.

Next, several existing designs will updated to the new technology in anticipation that they will be used to construct a first-order delta-sigma modulator. In most instances, the process parameters for each design will need to be updated and the circuit will be re-simulated. However, some of these designs may require more extensive modification including the recalculation some of the transistor aspect ratios. In addition, the layout of these designs will be scaled or modified to the design rules of the new minimum feature size. Due to the amount of work involved, in some instance it may easier to simply redraw an old design from scratch using the update design rules.

Finally, the updated designs will be used in conjunction with several new designs to create a first-order delta-sigma modulator. The ΣΔM will be constructed in pieces and ultimately the sections will be combined to form the completed circuit. It is anticipated that it will be necessary to create some sections of the circuit from scratch. New designs will be designed (schematic), simulated, drawn (layout) and sent to MOSIS for fabrication.

In addition to submitting a complete ΣΔM for fabrication, each part of the circuit will also be individually placed on a separate chip. In the event that the ΣΔM does not function as intended, it may be able to isolate the problem by testing each individual part.

2. EXPERIMENTAL PROCEDURE

2.1 Design Approach

The circuit design tools, Tanner Tools™, were used extensively in this project. The basic suite consists of five main tools that are used for the design, simulation, layout and verification of integrated circuits. Prior to the design of the ΣΔM, these tools must be updated to accept the new rules of the 0.5um process. Once corrected, the revised tools will be used to scale preexisting, 1.6um designs to the new 0.5um minimum feature size. New designs will be designed, simulated and tested using the approach illustrated in Figure 2.1.

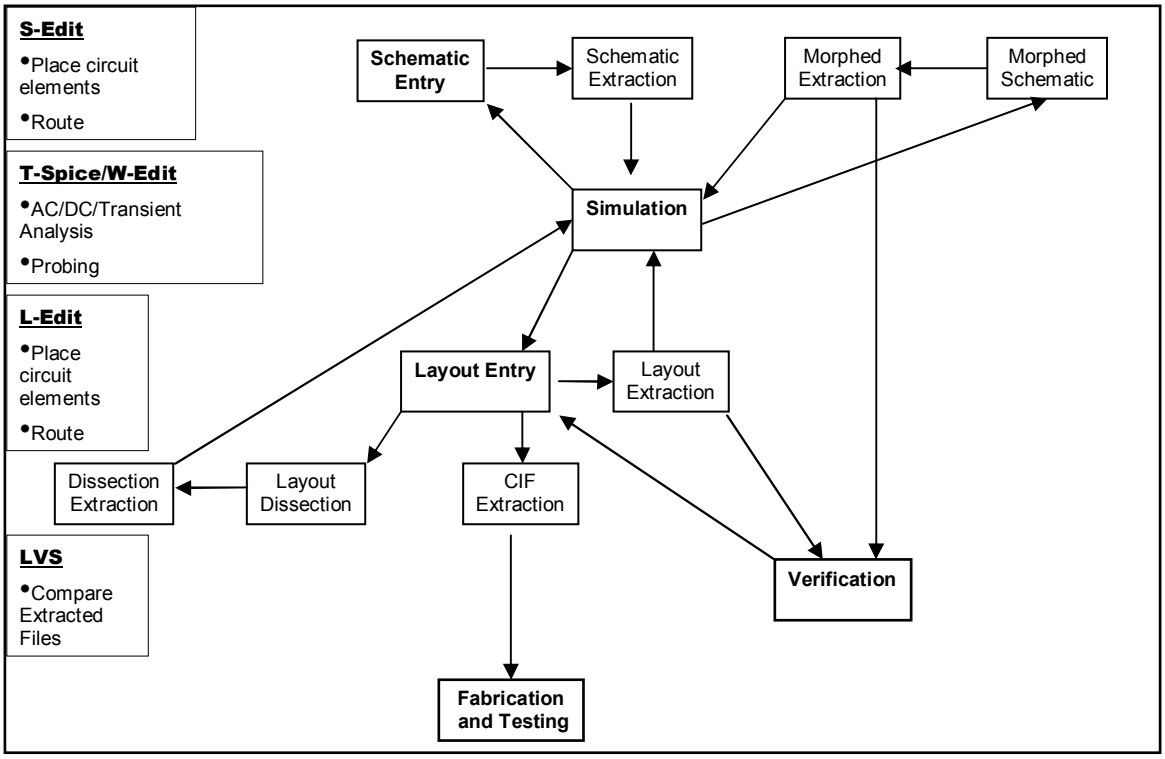

Figure 2.1: Design Flow

To start, new designs will be drawn using the schematic-entry tool, Tanner S-Edit™. Once the schematic is complete, a text-like representation of the circuit known as a SPICE file will be extracted. Next, during the simulation stage, Tanner T-Spice™ will be used to analyze the circuit SPICE file. If the circuit does not perform as expected, the

designer must return the design stage and revise the circuit schematic. If the circuit does perform as expected, the circuit design can progress to the layout stage.

During the layout stage, Tanner L-Edit™ is used to draw the masks that will be used to fabricate the circuit. After its completion, a SPICE file will be extracted from the layout for use in the circuit verification process. If any changes, such as breaking down large transistors into smaller pairs have been made to the layout, a new schematic (known as the morphed schematic) must be drawn, extracted and simulated.

Next, the layout and morphed schematic extraction files are compared using Tanner Layout-Versus-Schematic (LVS)™. The verification tool confirms that both circuits have the same number of elements and that they are both wired identically. If the verification tool finds any errors, then the circuit layout or morphed schematic must be corrected until both circuits are equal. As a final verification step, the circuit layout is extracted and simulated along with the pads that are connected to the pad frame. This step verifies that the circuit has been successfully connected to the pad frame. Finally, a CIF file can be extracted from the circuit layout and submitted for fabrication.

In accordance with this process, the individual parts of the ΣΔM will be designed, simulated and tested. Two separate designs have been submitted for fabrication. The first design contains individual parts of the ΣΔM that are wired to separate pads. This design allows each part of the circuit to be individually tested. The second design contains a complete, totally connected ΣΔM. After fabrication, each design will be bench-tested in the lab to verify the circuit's operation.

2.1.1 Design and simulation

The suite of circuit design tools, Tanner Tools™, was used for the design, simulation and layout of all circuits in this project. The Tanner Tools™ suite consists of four basic Tools; S-Edit™, T-Spice™ (and W-Edit™), L-Edit™ and LVS™.

Tanner Tools S-Edit™ is used for schematic entry. This tool allows a circuit schematic to be drawn with computer aid using preexisting circuit elements. Some of the

more common digital circuit elements and complete circuits are available in a library that is provided with the software. Once a schematic has been created in S-Edit™, T-Spice™ can be used to extract a SPICE deck and simulate the circuit. This powerful feature of the schematic entry tool allows a circuit to be easily visualized and analyzed.

An important feature of the schematic entry tool is its support for hierarchical circuit design. After a design has been drawn using basic circuit elements, the tool can be used to create a symbol for the design. The circuit symbol can then be "instanced" into larger designs. This feature can be used to simplify the verification process by breaking down complex circuits into smaller pieces.

Tanner Tools T-Spice™ is used for the simulation and analysis of circuits. The simulation tool aids in the design process by numerically solving the differential Equations that describe a circuit. The reader can refer to the T-Spice™ version 9.00 help file for information on the simulation process. In most instances, the simulation tool is used to simulate a circuit (SPICE deck) and W-Edit™ is used to display the simulation results graphically. The simulation tool supports several common types of simulations including AC, DC and transient analysis. Moreover, the simulation tool can be used in conjunction with S-Edit™ to probe a circuit for a more direct verification of a circuit's operation.

After a circuit has been designed and simulated, L-Edit™ is used to draw the circuit's layout. A layout is a representation of the actual masks that are used to fabricate an integrated circuit. The layout tool has a built-in design rule checker (DRC) that is used to verify that the circuit has been drawn according to a given set of process rules. Some examples of the rules that are checked are minimum layer sizes (width) and layer spacing. It is important to note that design rules are sometimes process dependent; that is, that certain design rules such as minimum width and spacing may vary for each process. The design rules must be modified in order to effectively scale or draw layouts using different minimum feature sizes.

An especially important feature of the layout tool is its ability to extract a SPICE deck from a layout. This feature aids greatly during the circuit verification stage. The layout tool it able to recognize certain circuit elements using a library of models. This library, known as the layout extraction file, must be updated to reflect the process change.

The last tool, LVS (Layout-Versus-Schematic)^{TM} is a verification tool that is used during the final stages of the circuit design. The verification tool is used to compare the SPICE file from the circuit schematic to the SPICE file from the circuit layout. Once executed, the tool looks for any discrepancies between the files. This tool is particularly helpful in isolating common errors such as layout (or schematic) problems or incorrect wiring. After the circuit's layout has been verified, a CIF or GDSII file can be extracted from the layout and submitted for fabrication.

2.1.2 Fabrication

Completed circuits are submitted to the MOSIS service for fabrication. This project is divided into two parts and was submitted to MOSIS as two separate designs.

The first chip was submitted under Alfred University's classroom account on an AMI C5 (0.5um) run. A MOSIS classroom account permits the fabrication of five parts, all packaged in DIP40 packages. This chip contained most of the basic parts of the ΣΔM including the folded-cascode op-amp, latched comparator and switched capacitor filter, but each part was individually wired to the pad frame. Several versions of each design were placed on the chip to ensure that any incorrect operation could not be a result of fabrication problems. It should also be noted that in the first design, the transistors of the switched capacitor were not drawn to minimum feature size.

The second chip was submitted for fabrication under an Alfred University research account on another AMI C5 (0.5um) run. A MOSIS research account requires that 40 chips be fabricated, however only five chips were placed in DIP40 packages. The remaining 35 chips are left unpackaged and for all intents and purposes are useless. This design contains several, individually wired parts (for individual testing) as well as a complete ΣΔM. Unlike the previous design, the transistors of the switched capacitor filter were redrawn to minimum feature size. This modification was necessary to allow the switched capacitor circuit to switch more quickly.

In each case, a pad frame that was obtained from the MOSIS service Web site was used for the design layout. The pad frame is illustrated in Figure 2.2.

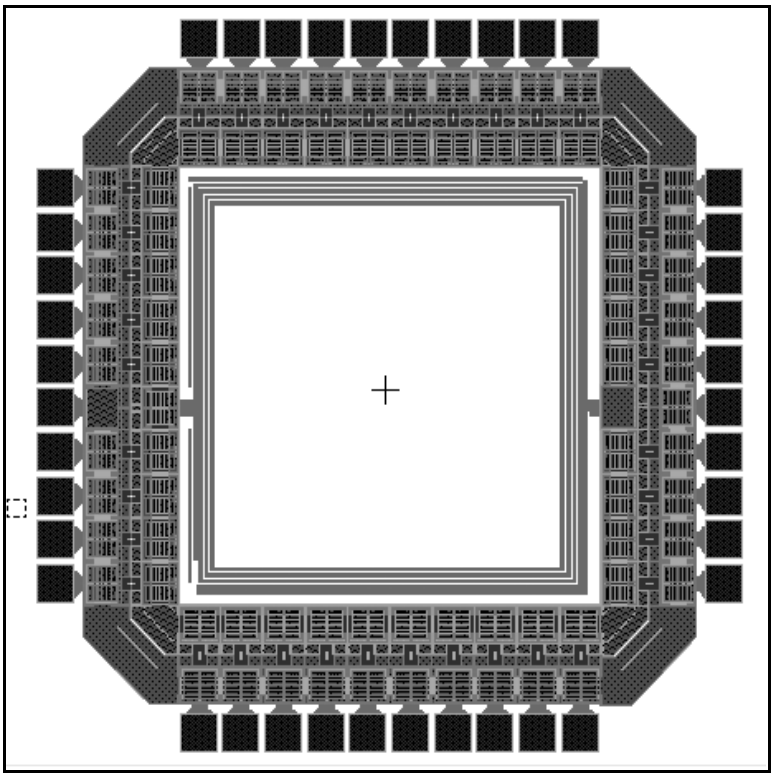

Figure 2.2: Pad Frame

Although it was designed for another process, the pad frame was successfully modified for use in the AMI 0.5um. This frame features some diode and over-voltage protection for the circuit inside. As illustrated, common signals were placed on rails that are wired to individual pads. This design approach minimizes the number of pads required to drive a design that uses many similar signals.

2.2 Process Transition

One of the primary objectives of this project was to upgrade Alfred University's circuit design tools to a newer process that utilizes a smaller minimum feature size. As IC fabrication technology advances, the minimum feature size of circuit designs become exponentially smaller. The most obvious advantage of this progression is that a smaller minimum feature size allows circuit designs to be fabricated using considerably less space on a wafer. In addition, the physical dimensions of the chip become smaller and allow the circuit to take up less space inside another electronic device such as a cell phone.

Along with these advantages, the circuit designer is presented with several new problems. The foremost problem is that existing circuit design tools must be updated to utilize the new minimum feature size.

2.2.1 Design rule modification

Most of the process upgrade work required that the layout editing tool, L-Edit™ be updated. The update process began by editing and appending the layout tool's design rules. Many of the design rules such as minimum layer width and minimum layer spacing were updated to reflect the process change. The most drastic changes to the design rules were poly1 minimum width, gate to well spacing and via1 spacing. The impact of these design rule changes appeared most prevalent when existing designs such as the folded-cascode op-amp were scaled to the smaller minimum feature size. In general, when modifying an existing design, the new rules required the following modifications:

- The removal of several via's from MOSFET gates, sources and drains.
- An increase in the distance between the via's of the gate and the via's of a source or drain.
- An increase in the minimum width of poly1.

Several other rules were modified and appended to the existing design rules; however, they had a much less noticeable effect. These changes become apparent by directly comparing the folded-cascode layout drawn in a lambda = 1.6um process (a) and a lambda = 0.5um process (b) is shown in Figure 2.3.

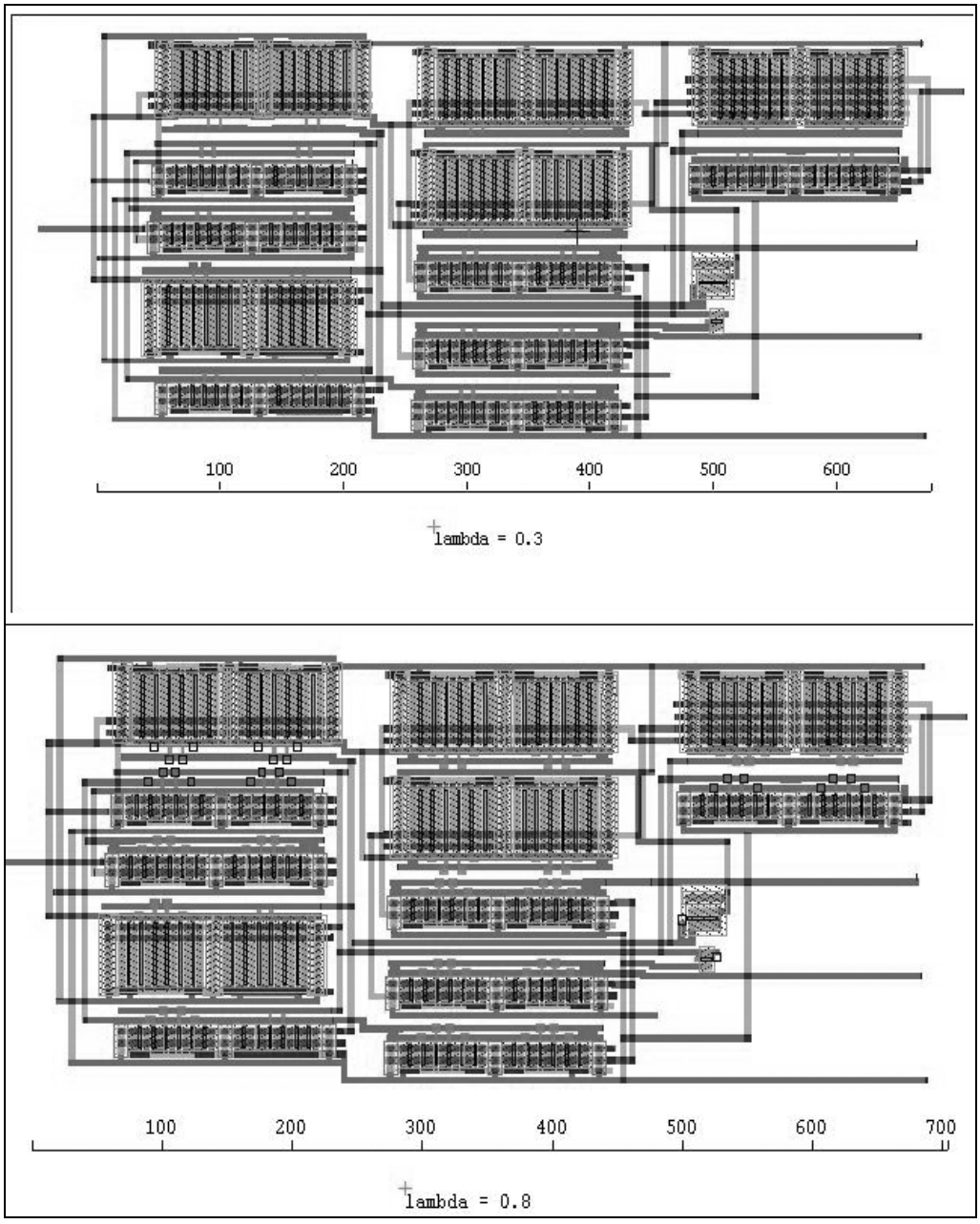

Figure 2.3: (a) Amplifier Drawn Using Lambda=0.3 (0.5um technology)
(b) Amplifier Drawn Using Lambda=0.8 (1.6um technology)

From the illustration, it is evident that each transistor needed to be increased in lambda units in order to accommodate for the change to poly1 and via spacing. A closer inspection reveals that the 0.5um circuit has fewer via's that are more widely spaced than the 1.6um circuit.

2.2.2 Layer/extraction file modification

An extraction file contains models that L-Edit uses to identify various circuit elements. Once recognized, these elements are converted to a SPICE script (netlist) which is later used for simulation and circuit verification. Each extraction file requires several statements to recognize a circuit element. These statements can be divided into two categories. The first set of statements specifies any electrical connectivity between layers. In other words, these statements tell the extractor which layers are connected (if they are able to be connected). An example of this type of statement is shown below:

connect(poly wire, AllMetal1, Poly Contact)

From this statement, the extractor is able to recognize that there is a connection if a poly contact is placed on overlapping layers of poly and metal1.

The second category of statements are known as model statements. Once the extractor has recognized that there is a connection between two or more layers, model statements are used to identify which circuit elements are formed by a given set of layers (if any). An example of a model statement is shown below:

```
# NMOS transistor with poly1 gate
device = MOSFET(
        RLAYER=ntran;
        Drain=ndiff,  AREA, PERIMETER;
```

Gate=poly wire;
Source=ndiff, AREA, PERIMETER;
Bulk=subs;
MODEL=NMOS;
)

As the comment (#) indicates, this model statement specifies the layers associated with a NMOS transistor with a poly1 gate. It can be observed that this type of transistor is formed by an n-type source and drain and poly gate.

A comparison of the 1.6um and 0.5um extraction files from an older HP process revealed that a majority of element models are similar, however several discrepancies were present:

- Layers "poly2" and "poly2 contact" were not present in the HP 0.5um extraction file or the L-Edit™ layer manger.
- Generated layer "poly2 wire" was not present in the L-Edit™ layer manager.
- Model "poly1-poly2 capacitor" was not present in the 0.5um extraction file.
- The connectivity statement for the layer poly2 is missing from the 0.5um extraction file.

The first two problems were easily corrected by adding layers "poly2" and "poly2 wire" to the L-Edit™ layer manager. Layer "poly2" was created by copying layer "poly" and updating the layer's CIF and GDSII numbers. Layer "poly2 wire" is a generated layer that is created during extraction and did not require a CIF or GDSII number.

The remaining problems were addressed by copying the following connectivity and model statements from the 1.6um extraction file to the HP 0.5um extraction file:

connect(poly2 wire, AllMetal1, Poly2 Contact)
 # Poly1-Poly2 capacitor
device = CAP(

RLAYER=Poly1-Poly2 Capacitor, AREA;
Plus=poly wire;
Minus=poly2 wire;
MODEL=;
)

The connectivity statement indicates that there is a connection if a poly2 contact is placed on overlapping layers of poly2 and metal1. The model statement allows the extractor to recognize that a capacitor is formed by overlapping layers of poly and poly2.

2.3 Simplified Schematic and Layout Approach

A majority of the design, layout and verification of the ΣΔM was completed within a six month timeframe. This was accomplished using specific schematic-entry and layout techniques that greatly speed up the design process. Some advantages of this expedited design approach include:

- *Quick turn around.* A circuit can be designed and fabricated within a small timeframe.
- *Simplified schematic-entry*. The expedited approach only uses a few transistors to create an entire circuit. Instead of creating several transistors with varying aspect ratios, the circuit is assembled using a few transistors with identical aspect ratios.
- *Simplified layout*. The use of identical transistors in the circuit schematic allows the circuit layout to be assembled using a few identical transistor pairs. In other words, after a layout has been created for a single transistor, the layout can simply be copied several times to form the complete circuit.

- *Faster verification times.* After a single transistor layout has been verified, each transistor of the complete layout is effectively verified. This can be attributed to the usage of identical transistors in the circuit layout a design.

Conventional design approaches require that each transistor of the circuit be individually designed. In each case, the square law model for transistors is used to calculate the transistor aspect ratio for a given current or transconductance requirement. In accordance with the expedited layout approach, one NMOS and one PMOS device are designed for usage in the entire circuit. Each transistor is drawn wide to allow for maximum current transfer.

Unfortunately, expedited design time comes at a cost. Some of the consequences of this approach include:

- *Wasted wafer space.* Wafer space is sacrificed in the interests of expedited design time. Some transistors which may have been created using a smaller aspect ratio are implemented using a "standard transistor pair." Consequently, some of the space on the chip is unnecessarily wasted.
- *Slew rate and switching time reduction*. This design approach requires that every transistor of a circuit be created from one NMOS and one PMOS pair. As a result, some transistors that could have been drawn using a smaller aspect ratio are actually drawn larger than required.
- *Low output swing*. Another consequence of this approach is that the circuit is not able to produce a very wide output swing. Part of this problem is a direct result of using a generic transistor for each transistor in the circuit. This technique does not allow the stages of the circuit to be properly matched.

Key techniques that were used in the expedited design process are outlined in the next few sections. In addition, several schematic-entry and layout methods which minimize common circuit problems such as noise and offset are discussed.

2.3.1 Schematic entry techniques

After a design has been simulated, the circuit designer must choose how to lay out the design on a chip. The layout of circuit is completely arbitrary; however there are several factors that should be taken into consideration.

First, large transistors should be broken up into several smaller transistors. A parallel set of small transistors can switch as effectively as a large transistor and produce the same amount of current. This technique is shown in Figure 2.4

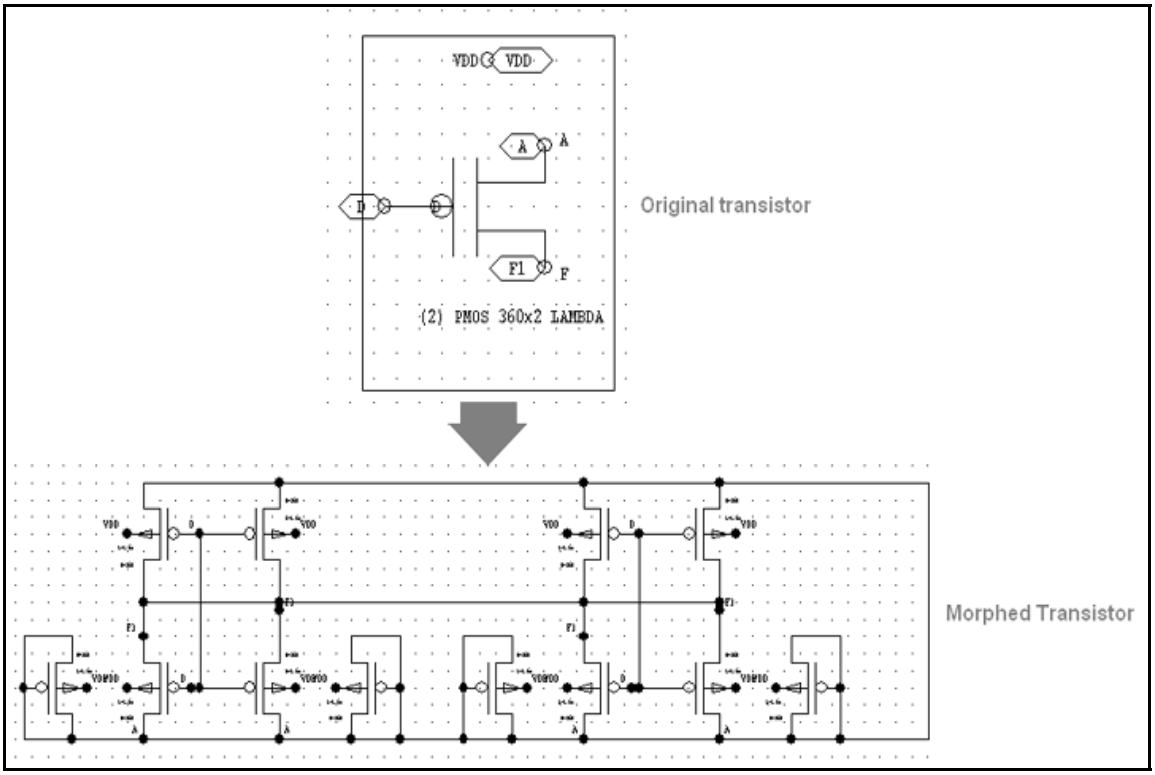

Figure 2.4: Transistor Morphing

As shown in the illustration, a very large PMOS transistor has been broken up into a smaller set of transistors. In this case, the design was broken up into eight identical transistors (with four dummy transistors). The gates, sources and drains of four to eight (depending on size) smaller transistors are connected parallel to one another. The aspect ratio of each transistor is identical so that each transistor produces the same amount of current and current flows through each transistor at the same rate. Large transistors are broken up into smaller pairs to decrease the size of the transistor channel. Many of the noise sources inherent to integrated circuits can be attributed to the usage of large transistors. When the gate and drain of a MOS transistor are connected, part of the channel will impede the flow of current, regardless of the doping purity. Eventually, the transistor will heat up and add thermal noise to any signal that passes through it.

Figure 2.4 also illustrates the usage of "dummy" transistor on each side of a transistor set. When a transistor is fabricated, sometimes the transistors that are located on the fringes of the wafer do not receive a deep etch or the optimal amount of doping. Consequently, fringe transistors may not operate as desired. The placement of "dummy" transistors ensures that the more crucial circuitry does not experience any of these fabrication problems. These transistors are referred to as "dummy" transistors because the gate, source and drain of each transistor are shorted out.

Next, the schematic is inspected for common pairs. A common pair is a set of transistors that have identical aspect ratios. By arranging transistors in pairs, the layout designer can effectively minimize the amount space that is being wasted on the chip. Furthermore, this layout technique allows transistors to be instanced more easily. Figure 2.5 illustrates this type of schematic entry approach.

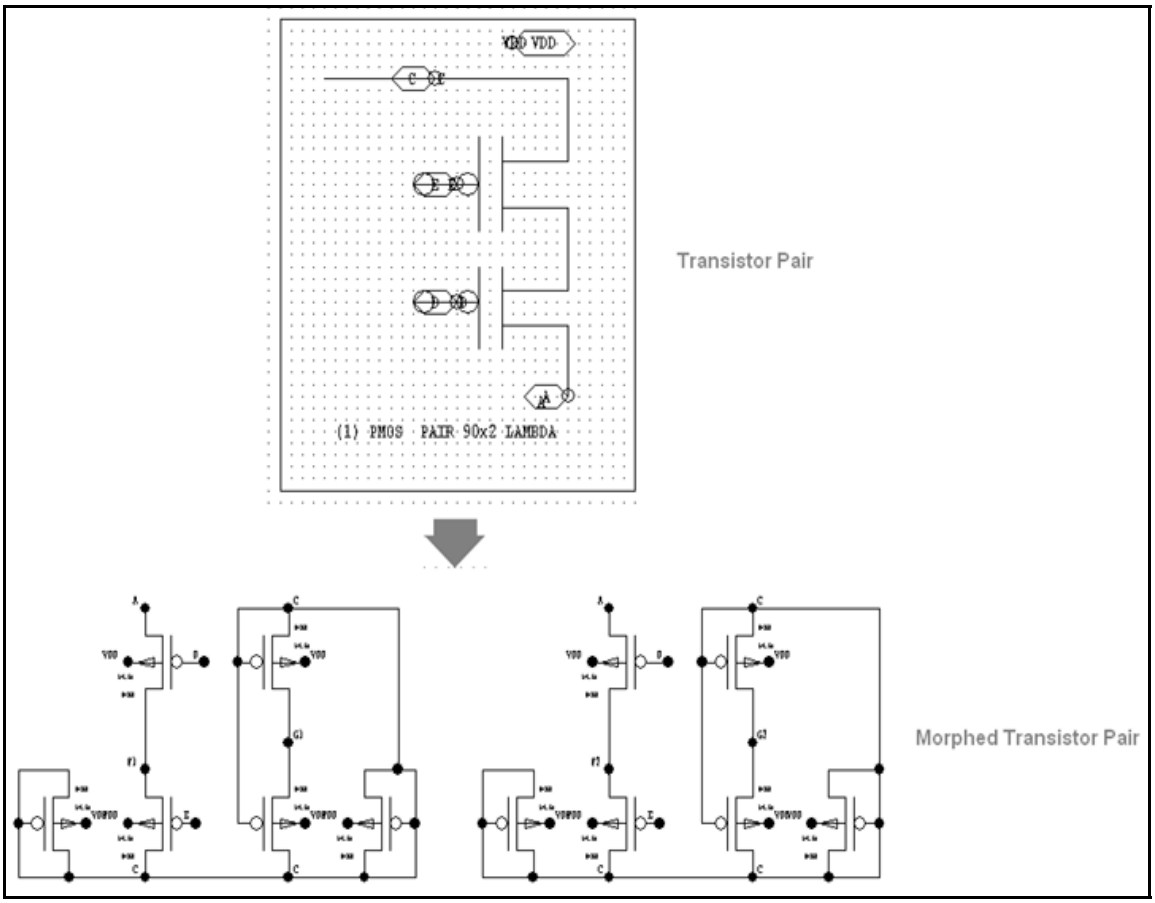

Figure 2.5: Common Pair Morphing

Transistors that are arranged in this configuration can later be drawn as a pair during the layout stage. The key difference between a common pair and the transistor shown in Figure 2.4 is that during the layout stage, a common pair can be laid out in one transistor block whereas the large transistor of Figure 2.4 uses an entire block. As a result, in the interests of space, it is desirable to arrange as many transistors as possible in a common pair configuration.

The entire layout process is described by Wei Lui in his Master's Thesis "Low Offset Operational Amplifier Design and Layout".[4] Here, Liu uses the "standard cell" approach to design a folded-cascode transconductance amplifier.

2.3.2 Morphed schematic creation

An important part of the verification process is the creation of a morphed schematic. When a SPICE file is extracted from a layout, the extractor will pull out every transistor in the layout, including dummy transistors and transistors that have broken up into smaller pairs. The extractor does not recognize that several transistors may be used in place of a larger transistor. Consequently, it is common for a circuit to appear different to the verification tool, especially when using the schematic-entry techniques described in this report.

If a single, large transistor has been broken down into several, smaller transistors, then a new schematic (known as the morphed schematic), must be created to reflect the change. In addition, any dummy transistors or other devices that were added to minimize fabrication errors must also be added to the morphed schematic. This approach will allow the verification tool to make an accurate comparison of the schematic and layout files.

2.3.3 Layout verification techniques

After the layout of circuit is complete, Tanner Layout-Versus Schematic (LVS) can be used to verify that the layout and morphed schematic are equal. Once executed, the program reads and compares the SPICE file from the circuit schematic and the layout. The program verifies that both SPICE files are wired the same and that they have the same number of devices and nodes.

If the circuit passes an LVS test, it can be connected to the pad frame. Any circuit terminals that require an isolated pad are wired accordingly while other more universal terminals (such as VDD or GROUND) are wired to rails. By placing commonly used connections on a rail, the circuit designer can effectively minimize the use of pads and extra wires.

The final stage of the verification process is called “dissection.” A circuit dissection verifies that the circuit has been correctly wired the pad frame and that no critical errors, such as missing via’s, have been made. Figure 2.6 illustrates the dissection process.

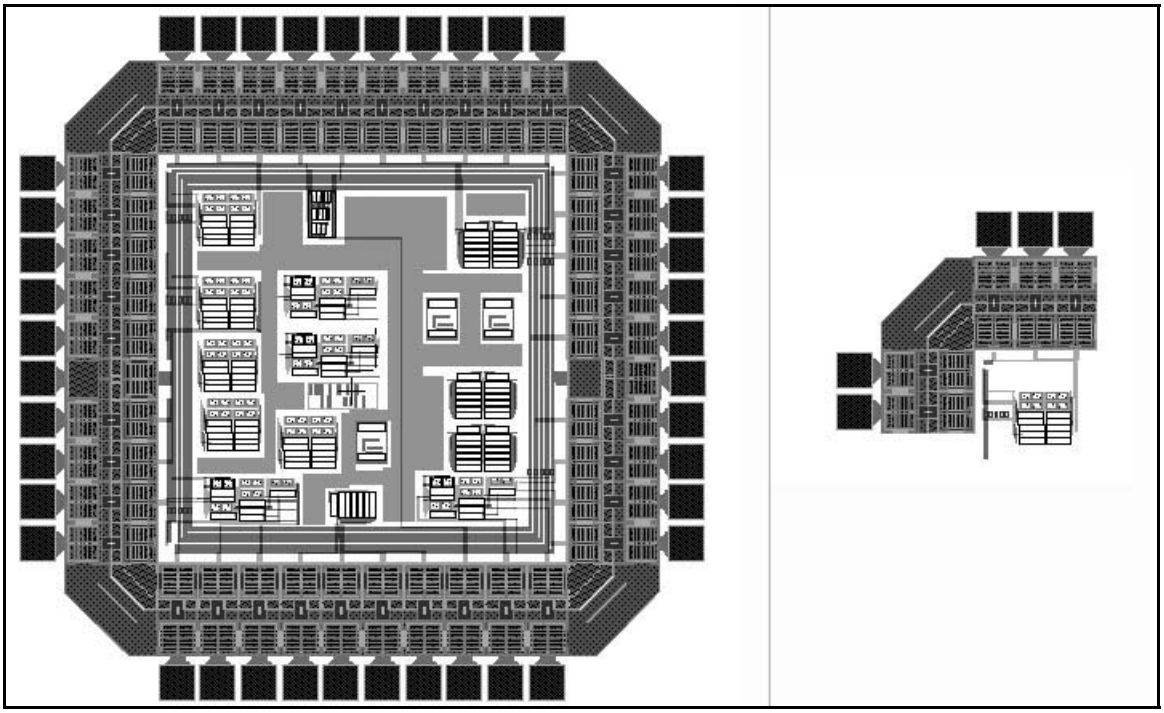

Figure 2.6: (a) Whole Circuit
(b) Dissected Circuit

As Figure 2.6 illustrates, the dissection process involves extracting a single part of the circuit along with any pads that are connected to it from the complete layout. Next, a SPICE file can be extracted from the dissected layout and simulated using T-Spice™. When simulated, all the input signals should be applied to the input pads of the circuit and any output should be read from the output pads. In general, these simulations will not produce desirable output due to the extra circuitry inside the pads that cannot be SPICE simulated. However, if the simulation produces some output, then it can be assumed that the circuit has been correctly wired to the pad frame.

2.4 Operational Amplifier Design

The operational amplifier (op-amp) currently is the industry standard for high gain devices. Ideally, an op-amp circuit has a high gain, low output resistance and is able to handle high impedance signals.

While the design of an op-amp circuit can vary, the basic premise behind each stage of the op-amp is usually the same. The first stage of the op-amp is designed to handle a large input resistance. The second stage, usually a difference mode amplifier, provides high gain. The final stage lowers the output resistance of a signal. It is these properties that make the op-amp ideal for many small signal applications. The symbol commonly used for an operational amplifier is shown in Figure 2.7.

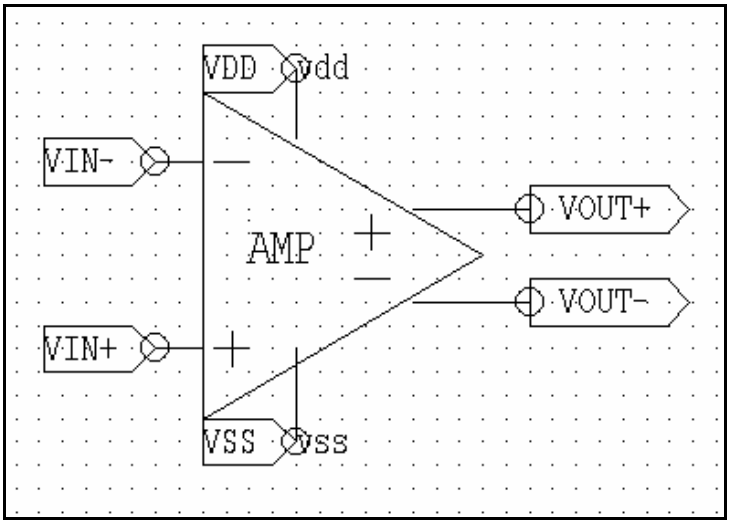

Figure 2.7: The Operational Amplifier

As illustrated, most op-amps have two inputs and two outputs. The terminals, VSS and VDD provide DC voltage for the circuit. The outputs of the op-amp (VOUT+, VOUT-) are balanced such that the output of the non-inverting terminal (VOUT+) is the inverse of the inverting terminal (VOUT-).

In an ideal situation, the output of the amplifier is dependent on the differential input voltage (V_d). As shown in Equation 2.4.1, the differential input voltage is defined as the difference between the inverting and non-inverting input voltages.

$$V_d = (V_{in+} - V_{in-}) \quad \textbf{(2.4.1)}$$

Where V_{in+} and V_{in-} are the inputs of the amplifier. The output of the amplifier can be calculated by multiplying the gain of the amplifier by differential input voltage. This relationship is show below:

$$V_o = A_V (V_{in+} - V_{in-}) \quad \textbf{(2.4.2)}$$

Where V_o is the output voltage and A_V is the gain of the amplifier.

Another important characteristic of an op-amp is its slew rate (SR). The slew rate of an amplifier is a measure of the amplifiers ability to switch from its maximum output voltage to its minimum output voltage. This relationship is shown in Equation 2.4.3.

$$SR = \frac{\Delta V}{\Delta T} = \frac{(V_{\max} - V_{\min})}{(T_1 - T_2)} \quad \textbf{(2.4.3)}$$

Where V_{max} and V_{min} are in the maximum and minimum output voltages, T_1 is the time at which the output begins to fall from V_{max} and T_2 is the time at which the output reaches V_{min}. This concept can be more clearly illustrated by examining the output of an amplifier as shown in Figure 2.8.

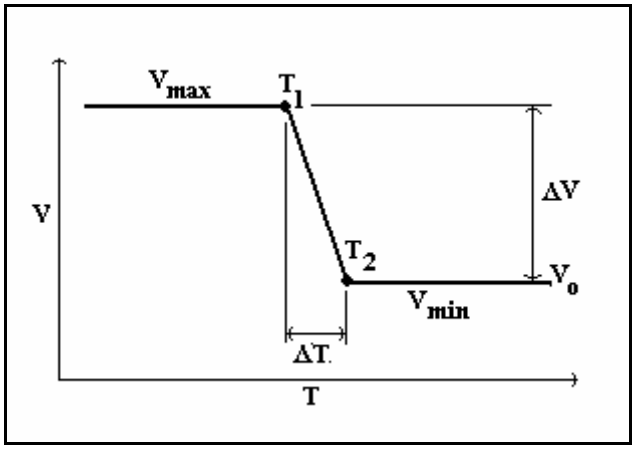

Figure 2.8: Amplifier Slew Rate

Circuit analysis tools such as T-Spice™ can be used to approximate a circuit's slew rate. Unfortunately, past experience shows that a simulation tool can at best, give a rough estimate. To obtain an accurate slew rate measurement, the circuit must be fabricated and bench-tested in the lab.

2.4.1 Design requirements

In this experiment, the operational amplifier is one of the fundamental building blocks of the switched capacitor filter. The rigors of analog to digital conversion demand that the amplifier be able to achieve high gain and have a fast slew rate. During the initial development stages of the ΣΔM, a two stage op-amp architecture was implemented. While this amplifier was able to satisfy the necessary gain requirements, it was not able to meet the slew rate requirements required for analog to digital conversion. Consequently, a folded-cascode, transconductance amplifier, which was proposed by Johns and Martin,[11] was utilized for the design of the ΣΔM. The folded-cascode amplifier is illustrated in Figure 2.9.

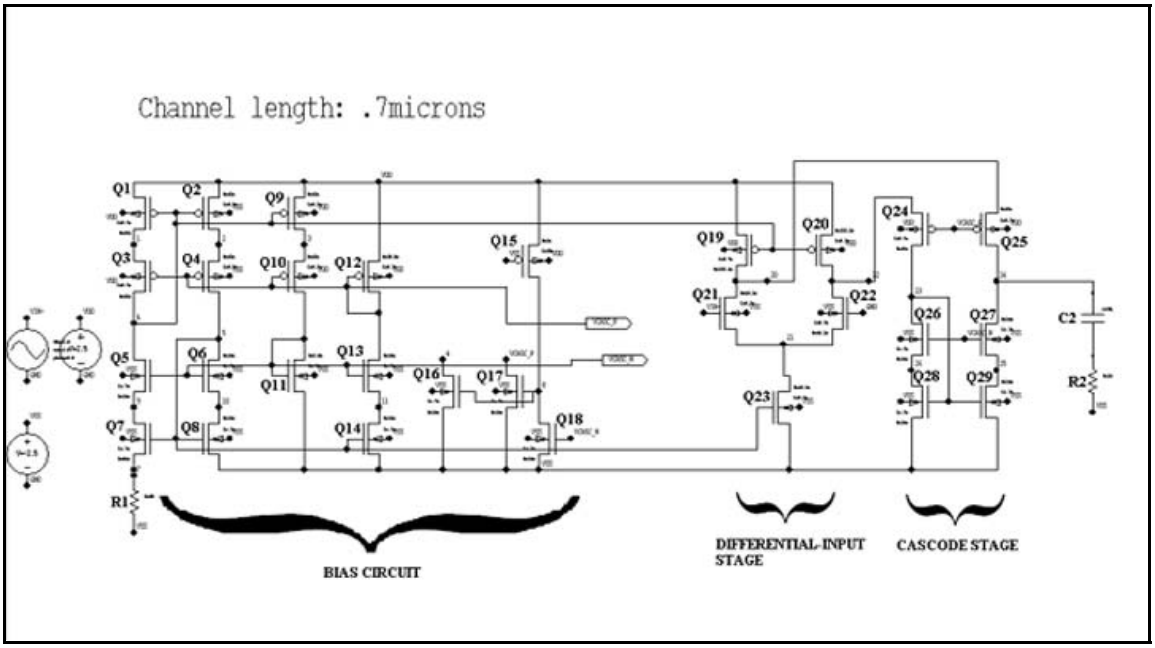

Figure 2.9: Schematic of the Folded-Cascode Operational Amplifier

The folded-cascode amplifier can be broken down into three distinct stages. The front-end of the circuit primarily consists of bias circuitry. The bias circuit utilizes wide swing current mirrors that provide very predicTable and sTable transconductances[11]. This modification greatly reduces most of the second order imperfections caused by the finite output impedance of the transistors without greatly restricting the output swing of the amplifier.

The next stage of the amplifier is known as the differential input stage. This stage's primary function is to provide gain. The differential input voltages are applied to the gate each NMOS, Q21 AND Q22 at VIN+ and VIN-. NMOS Q23 controls the amount of current that is allowed to flow into each leg of the amplifier. The output of the differential input stage is taken from each leg of the amplifier and then it is further amplified by the cascode stage. It is important to note that the input transistors of the cascode stage are the antithesis of output transistors of the differential input stage. This arrangement of opposite transistors type transistors allows the output of this single-gain stage amplifier to be taken at the same bias-voltage levels as the input signals. Consequently, the amplifier is able to achieve high gain because the gain determined by the product of the input transconductance and output impedance[12].

Table (I) shows the aspect ratios used in the simulation of the folded-cascode amplifier. As illustrated, these aspect ratios were borrowed from a 0.7um process simulation. In each case, the length of each transistor was left at the minimum feature size while the width of each transistor varies according to its specific current requirement.

Table I: Folded-Cascode Amplifier Aspect Ratios

Transistor	*Q1*	*Q2*	*Q3*	*Q4*	*Q5*	*Q6*	*Q7*	*Q8*	*Q9*	*Q10*	*Q11*
Aspect Ratio (W/L in um's)	42 / 0.7	42 / 0.7	42 / 0.7	42 / 0.7	14 / 0.7	14 / 0.7	56 / 0.7	14 / 0.7	42 / 0.7	42 / 0.7	3.5 / 0.7

Transistor	*Q12*	*Q13*	*Q14*	*Q15*	*Q16*	*Q17*	*Q18*	*Q19*	*Q20*	*Q21*	*Q22*
Aspect Ratio (W/L in um's)	10.5 / 0.7	14 / 0.7	14 / 0.7	20 / 2	14 / 0.7	14 / 0.7	14 / 0.7	132.2 / 0.7	132.2 / 0.7	44.1 / 0.7	44.1 / 0.7

Transistor	*Q23*	*Q24*	*Q25*	*Q26*	*Q27*	*Q28*	*Q29*
Aspect Ratio (W/L in um's)	44.1 / 0.7	42 / 0.7	42 / 0.7	14 / 0.7	14 / 0.7	14 / 0.7	14 / 0.7

An experimental approach was used to ascertain which amplifier could meet the slew rate requirements of the ΣΔM. The slew rate of several amplifiers that were previously fabricated using 1.6um technology was measured in the lab and compared. Bench-testing showed that the folded-cascode amplifier had the highest slew rate.

2.4.2 Morphed schematic of the folded-cascode op-amp

To efficiently lay out the transistors of the folded-cascode amplifier, similar transistors were divided into groups. Also, in the interest of noise minimization, large transistors were broken down into smaller transistor sets. As a general rule of thumb, each set contained twelve transistors; eight active transistors and four dummy transistors. If a transistor is especially large, then it may have required the use of all eight transistors. Smaller, common pairs of transistors were broken down into groups of four active transistors as outlined in the schematic entry section.

Figure 2.10 illustrates the completed morphed schematic for the folded-cascode amplifier. As the illustration shows, some transistors were not able to be paired.

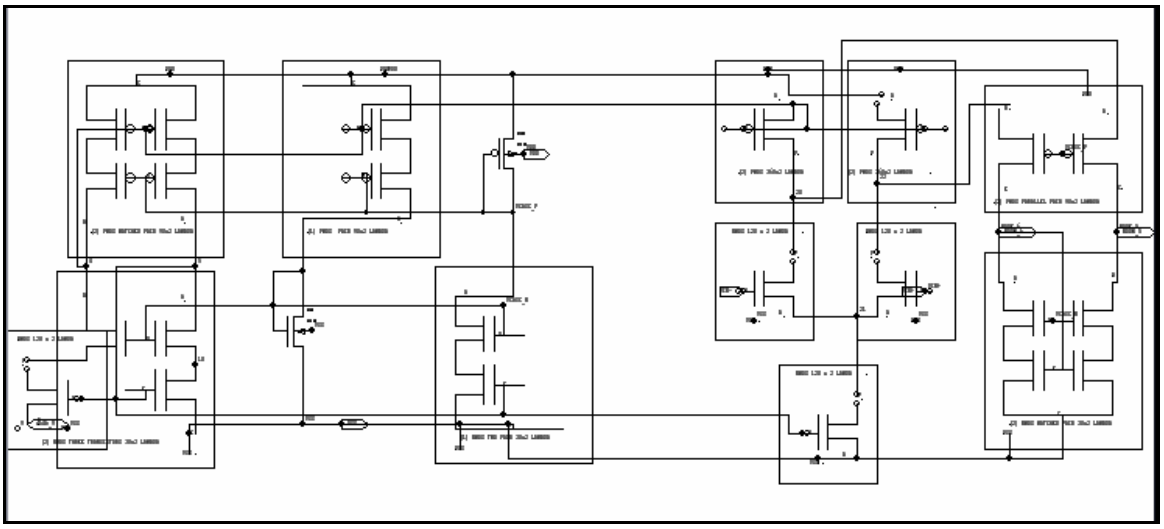

Figure 2.10: Morphed Schematic of the Folded-Cascode Op-amp

2.4.3 Layout of the folded-cascode op-amp

The layout of the folded-cascode amplifier was previously created by Dr. Wallace Leigh, for use in an AMI 1.6um. It was necessary to scale each transistor set for use in the 0.5um process. Figure 2.11 shows that completed layout of the folded-cascode amplifier.

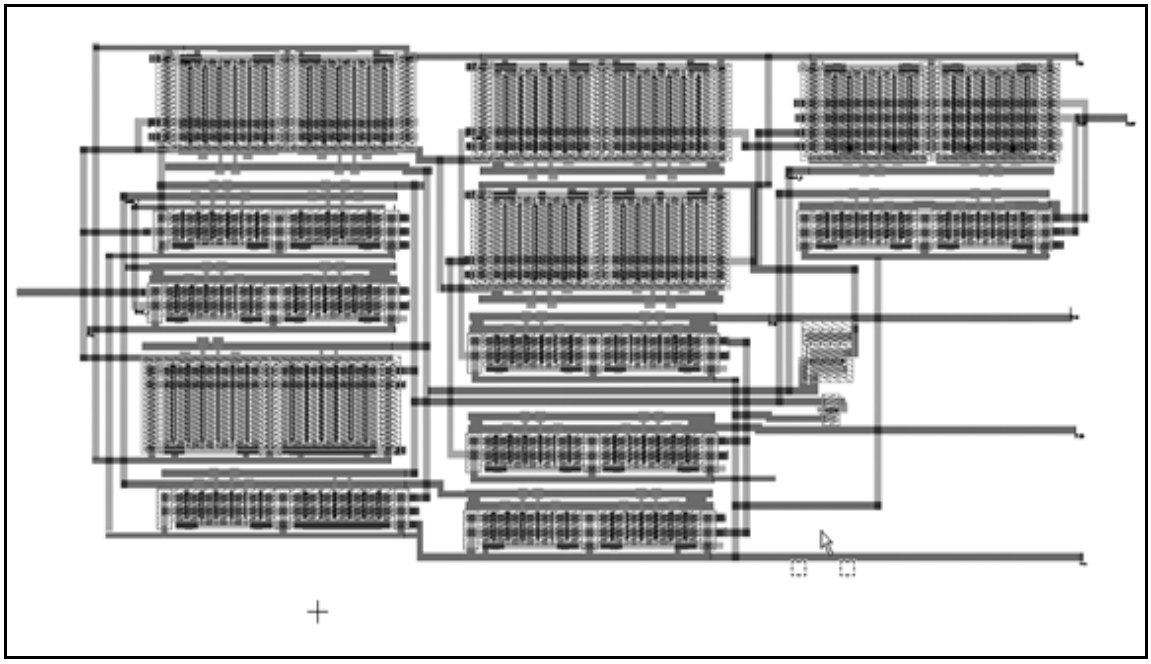

Figure 2.11: Folded-Cascode Op-amp Layout

Each transistor set has been assigned a name that corresponds to a transistor set in the circuit schematic. This allowed transistor sets to be compared quickly and easily if any problems were detected during the verification process.

2.5 Switched Capacitor Circuit Design

Conventional circuit design utilizes a resistor parallel to a capacitor to filter out high frequencies. However, due to the space constraints of VLSI, it is not practical to use passive components in a layout.

A switched capacitor filter circuit has the ability to filter high frequencies and also requires less space on a chip. It is due to these desirable characteristics, that the switched capacitor filter is widely used in analog electronics. A simple switched capacitor filter can be constructed using several, easily integrated components. The schematic for a simple switched capacitor filter is shown in Figure 2.12.

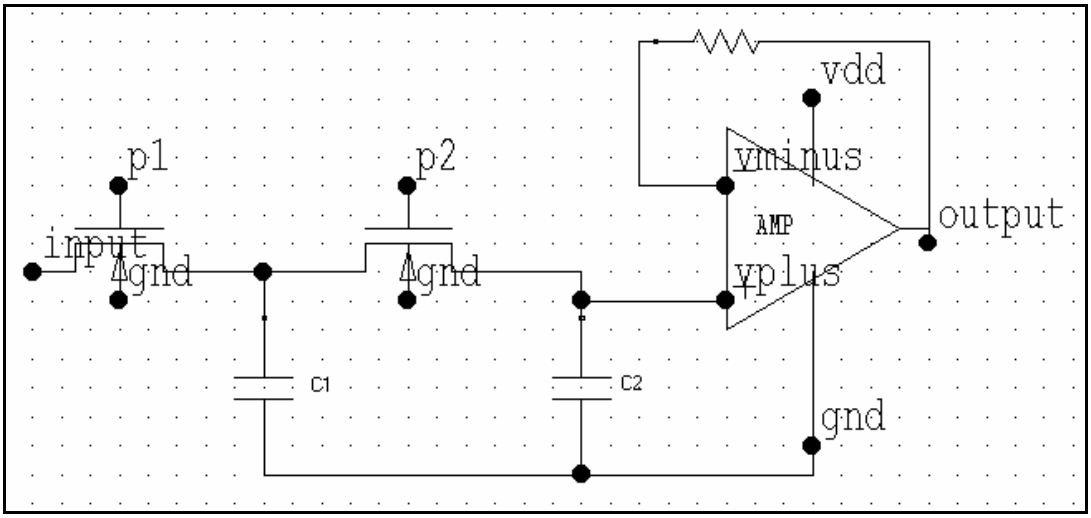

Figure 2.12: Switched Capacitor Filter

Figure 2.12 illustrates that a simple switched capacitor filter can be constructed by connecting two NMOS devices and two capacitors to the non-inverting side of the operational amplifier. A small resistor (off chip) provides feedback between the inverting side of the amplifier and the output.

The operation of the circuit can be described by studying the filter's response when a voltage is applied to p1 and/or p2. When a voltage is applied at p1, the charge (Q_1) is equivalent to the product of the capacitance (C_1) and the input signal, V_{IN} (or input). Therefore, the charge (Q_{OUT}) is equivalent to the product of the capacitance C_2 and V_{OUT} because an open circuit exists between C_1 and C_2. These relationships are defined in Equations 2.5.1 and 2.5.2.

$$Q_1(\phi) = Q_1(n-1) = C_1 V_{in} \qquad \textbf{(2.5.1)}$$

$$Q_{OUT}(\phi_1) = Q_2(n-1) = C_2 V_{OUT} \qquad \textbf{(2.5.2)}$$

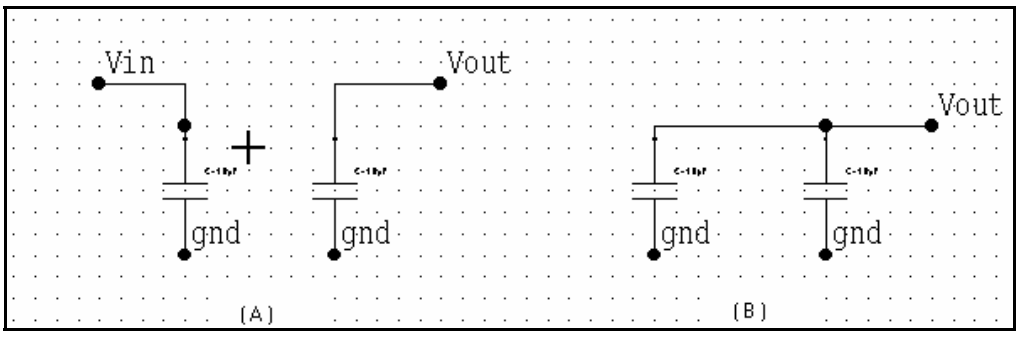

Figure 2.13: Switched Capacitor Filter Operation

Figure 2.13 illustrates the response of the circuit when a voltage is applied to the gate p2. Under these conditions, the NMOS (p2) creates a short between capacitors C_1 and C_2. The charge of p2 can than be expressed as:

$$Q_{OUT}(\phi_2) = Q_{OUT}(\phi_1) + Q_{IN}(\phi_1) = Q_{OUT}(n-1) + Q_{IN}(n-1) \qquad \textbf{(2.5.3)}$$

From Figure 2.13 (B) it is seen that Equation (2.5.3) can be rewritten as:

$$Q_{OUT}(\phi_2) = Q_{OUT}(n) = (C1 + C2)V_{OUT}(\phi_2) = (C1 + C2)V_{OUT}(n) \qquad \textbf{(2.5.4)}$$

Rewriting Equation (2.5.4) and solving for $V_{OUT}(n)$ yields:

$$V_{OUT}(n) = \frac{C2}{C1 + C2}V_{OUT}(n-1) + \frac{C1}{C1 + C2}V_{IN}(n-1) \qquad \textbf{(2.5.5)}$$

Next, the transfer function of the filter can be found by taking the z-transform of $V_{OUT}(n)/V_{IN}(n)$. This relationship is defined by $H(Z)$ as shown in Equation (2.5.6).

$$H(Z) = \frac{1}{(1+\alpha)} \bullet \frac{1}{Z - \frac{\alpha}{1+\alpha}} \qquad \textbf{(2.5.6)}$$

Where $\alpha = C2/C1$ and $Z = e^{j\omega T}$.

To find the 3db point of the circuit, *H(Z)* must be rewritten for when $Z = e^{j\omega T}$ and

$$H(Z) = \frac{1}{\sqrt{2}}.$$

$$\frac{1}{\left[1 + 2\alpha(H\alpha)(1 - \cos\omega_3 T)\right]^{\frac{1}{2}}} = \frac{1}{\sqrt{2}} \qquad \textbf{(2.5.7)}$$

Solving Equation (2.5.7) for the 3db point yields:

$$\omega_3 = 2\pi f_3 T \qquad \textbf{(2.5.8)}$$

which is the corner frequency for the switched capacitor.

2.5.1 Design requirements

The key to creating an effective, responsive filter is the selection of a suiTable operational amplifier. In general, the speed of the entire circuit is controlled by the amplifiers ability to slew quickly. As previously discussed, a folded-cascode amplifier was implemented to achieve the slew rate requirements of the ΔΣM.

At its inception, a single-sided switch configuration was used for the implementation of the filter. The single sided switch capacitor implementation is shown in Figure 2.14.

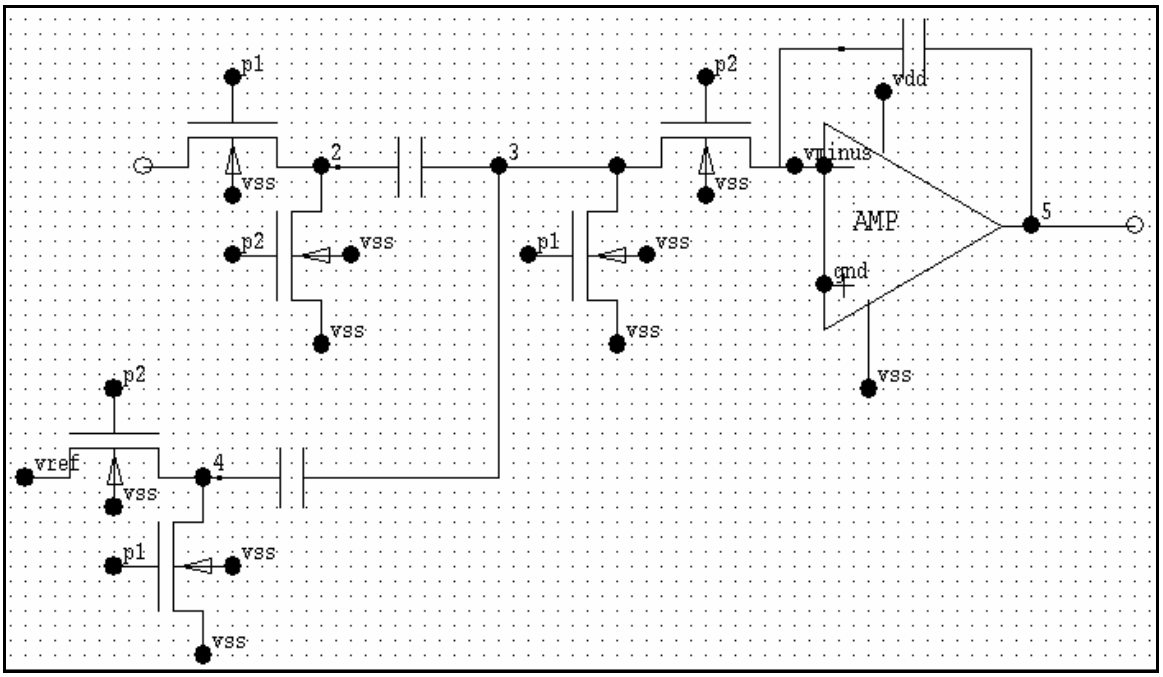

Figure 2.14: Single-Sided Switched Capacitor Filter

As the project progressed, it became evident that the ΣΔM required additional feedback in order to function correctly. Consequently, the double-sided, balanced output configuration proposed by Boser[13] was used for the filter implementation. The Boser filter is shown in Figure 2.15.

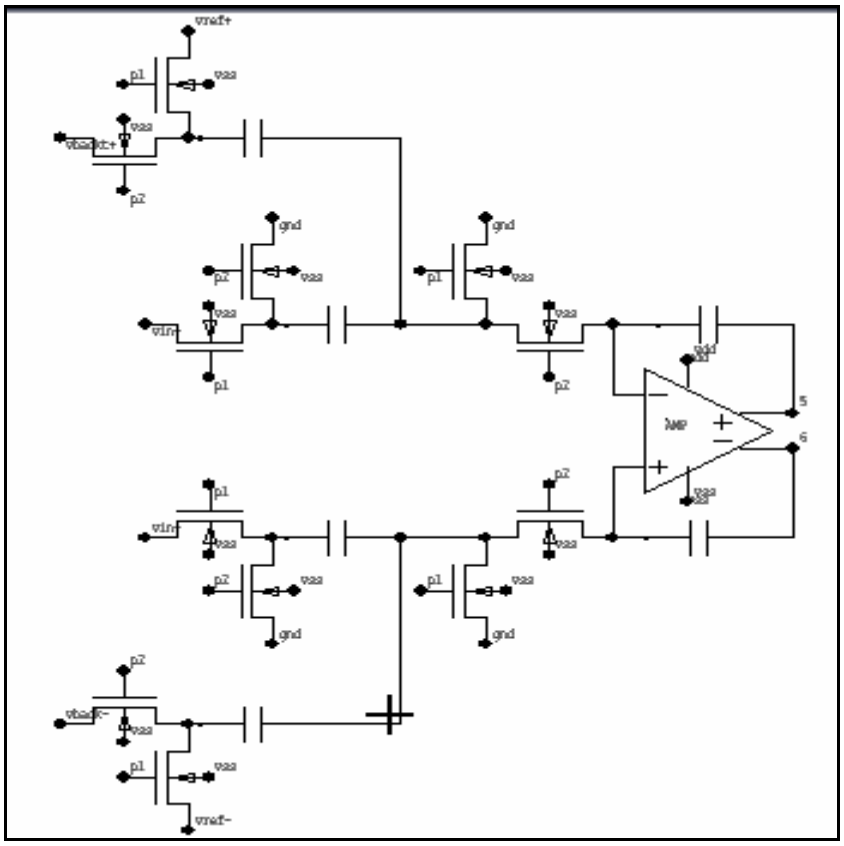

Figure 2.15: Boser Switched Capacitor Filter

Fundamentally, the Boser filter is very similar to a traditional switched capacitor filter. However, the filter has several key difference including a feedback loop and double-sided, balanced outputs.

From Figure 2.15, it can be seen that the inverting output of the filter is fed back into the non-inverting input of the amplifier through a series of switches. Conversely, the non-inverting output of the filter is fed back to inverting input of the amplifier. This configuration greatly increases the stability of the circuit. In addition, the feedback loop of each side of the circuit can be adjusted by varying the reference voltage, vref+ and vref-. This feature allows for noise and offset correction.

2.5.2 Morphed schematic of the switched capacitor

The layout of the switched capacitor filter was approached in two different ways. For the first method, transistors pairs from the folded-cascode amplifier were used for all NMOS switches. This approach allowed the layout and morphed schematic to be created quickly because a majority of the layout and schematic was already complete. Unfortunately, this architecture did not promote speed because of the large size of the switches. As a result, all NMOS switches were redrawn to minimum feature size. The transistor aspect ratios are shown in Table (II).

Table II: Switched capacitor aspect ratios

Transistor	Q1	Q2	Q3	Q4	Q5	Q6
Aspect Ratio (W/L in um's)	0.9 / 1.8	0.9 / 1.8	0.9 / 1.8	0.9 / 1.8	0.9 / 1.8	0.9 / 1.8

The morphed schematic of the switched capacitor filter is shown in Figure 2.16

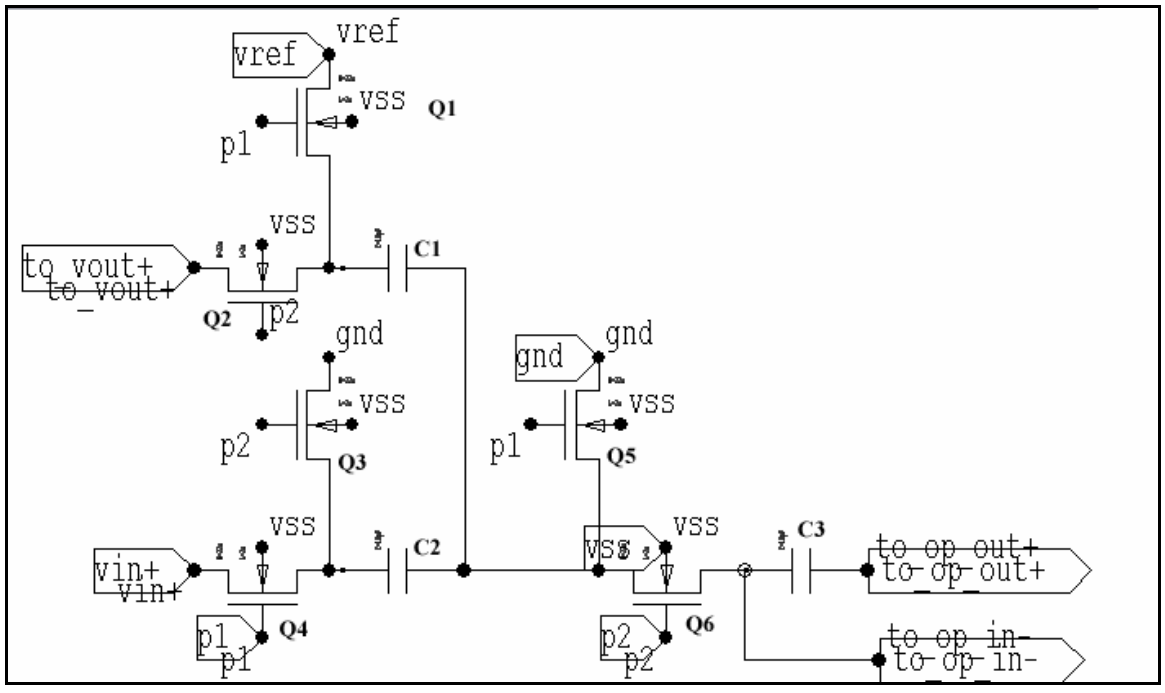

Figure 2.16: Morphed Schematic of Switched Capacitor Filter Leg

As illustrated, both sides of the filter are identical. Therefore, it was only necessary to create a schematic for one side of circuit. Once drawn, the switched capacitor leg was copied and combined with the morphed schematic of the folded cascode amplifier to form the complete morphed schematic. The complete morphed schematic is shown in Figure 2.17.

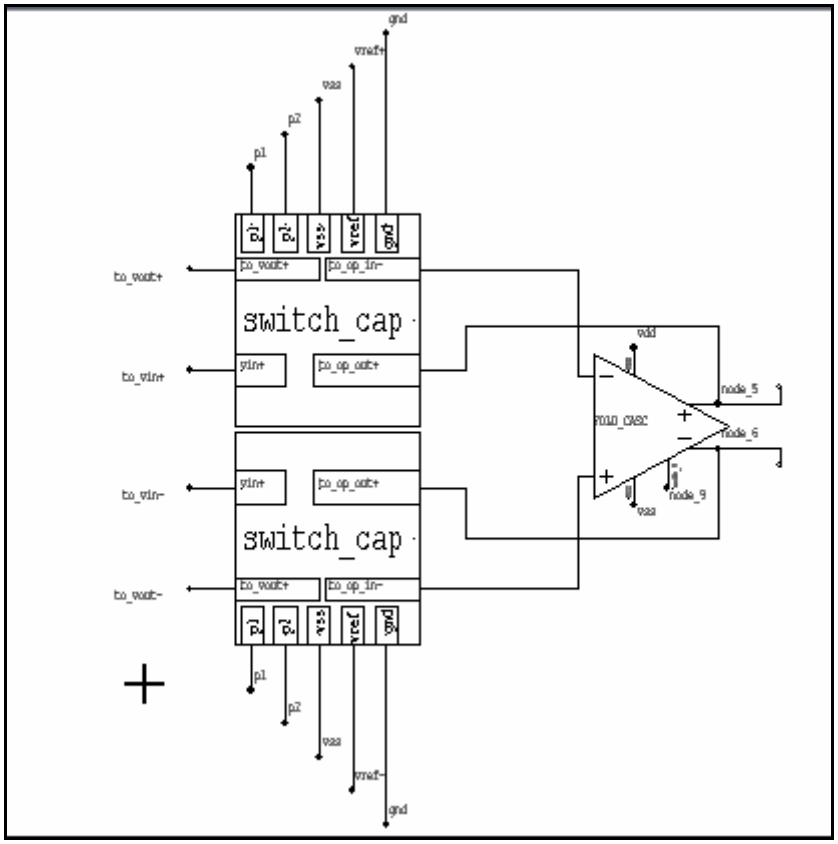

Figure 2.17: Complete Morphed Schematic of Switched Capacitor

As shown in the illustration, a symbol was drawn for each leg of the switched capacitor and combined with the folded-cascode amplifier. In addition to the normal terminals required to drive the circuit, vref+ and vref- were pulled out of the schematic to allow for "fine tuning" at a later time.

2.5.3 Layout of the switched capacitor

The aspect ratio of the capacitors can be determined using the SPICE parameters on MOSIS's Web site. First, an average of the inter-layer capacitance (per unit area) between poly1 and poly2 was taken from several AMI 0.5um runs. Next, if the desired capacitance is known, then the area of the capacitor can be determined by dividing the capacitance by the inter-layer capacitance. If the capacitor is square, then the aspect ratio of the capacitor can be determined by taking the square root of the capacitor area

The capacitor aspect ratios are shown in Table (III) below. An inter-layer capacitance of 869 aF/um^2 was used for each calculation.

Table III: Capacitor Aspect Ratios for Switched Capacitor Circuit

Capacitor	*C1*	*C2*	*C3*
Capacitance (pF)	0.6	0.6	1
Area (um^2)	691	691	1151
Width (um)	26	26	34
Length (um)	26	26	34

Figure 2.18 illustrates the preliminary layout of the switched capacitor circuit. This configuration utilizes a small NMOS pair from the layout of the folded cascode amplifier. In this design, the layout of the folded-cascode amplifier has been excluded from the circuit.

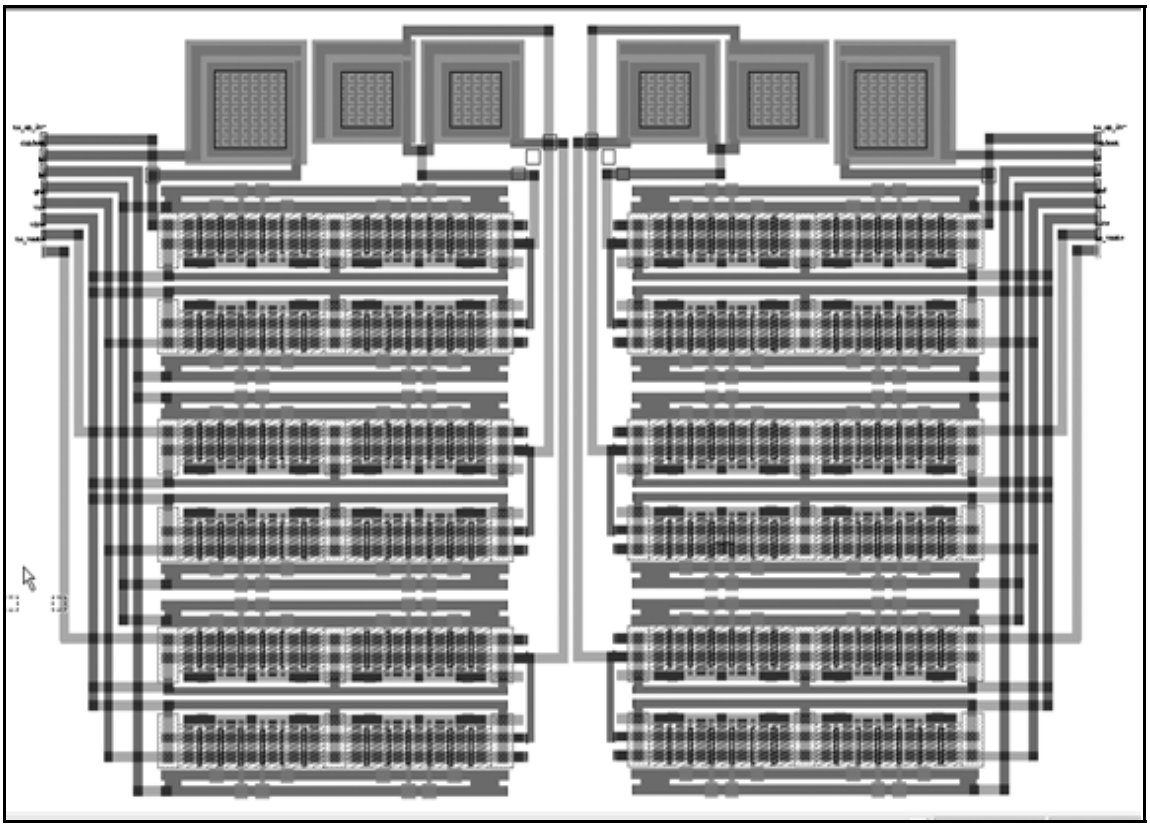

Figure 2.18: Preliminary Layout of the Switched Capacitor

While the preliminary layout of the filter may have been totally functional, in the interests of speed, it was decided to redraw the switches of the circuit. The switching rate of the circuit is effectively increased by redrawing the switches to minimum feature size. The capacitors from the preliminary layout were also used in this layout. The new, faster switched capacitor filter is shown in Figure 2.19.

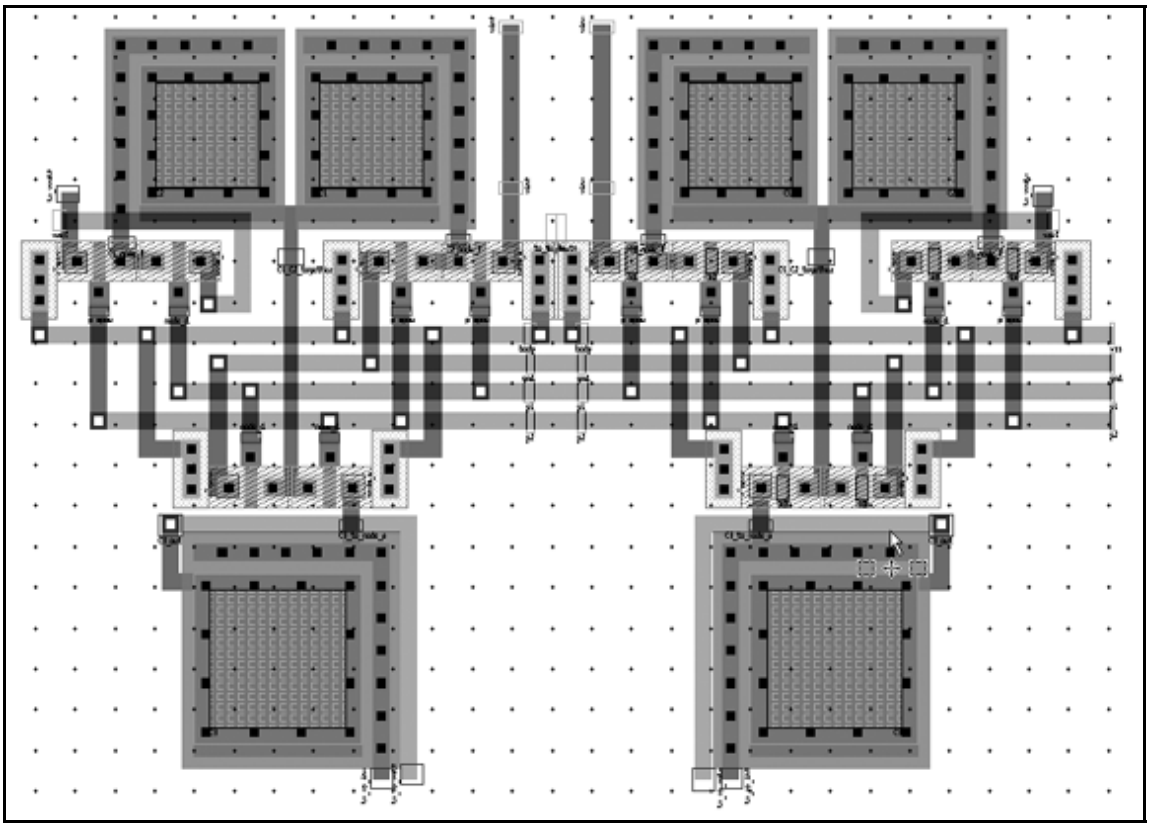

Figure 2.19: Revised Switched Capacitor Circuit

Like the preliminary schematic, vref+ and vref- were individually connected to pads to allow for "fine tuning." The completed switched capacitor filter was wired to the folded-cascode amplifier as shown in Figure 2.20. All common signals such as VDD and VSS were connected to minimize the amount of pads required for the design.

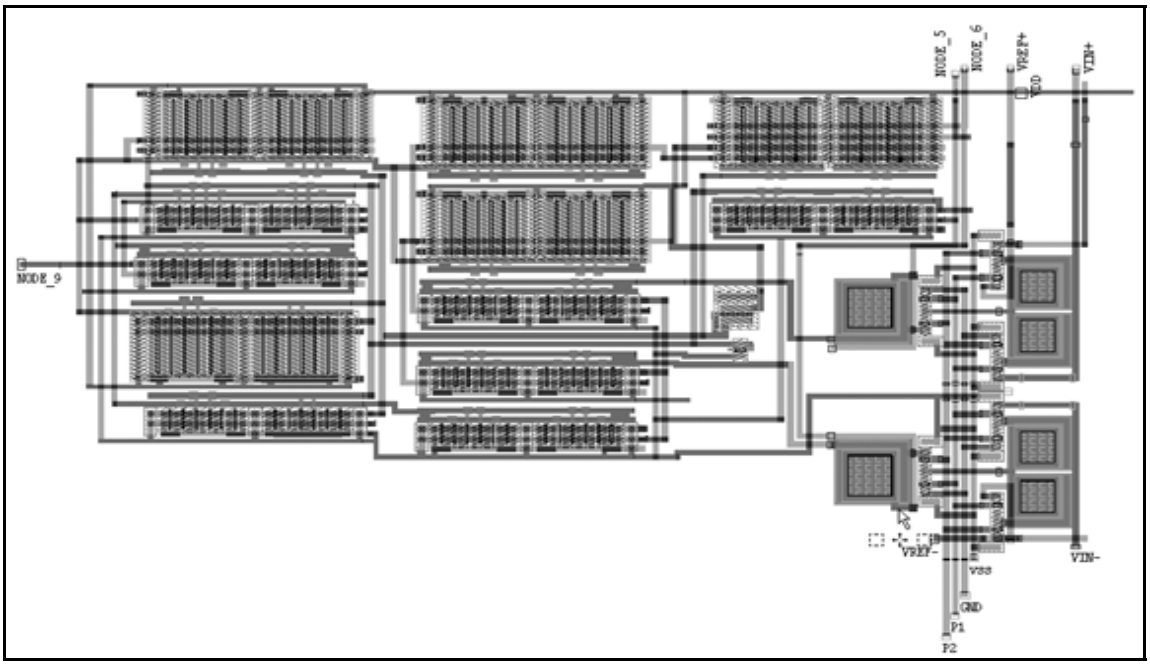

Figure 2.20: Complete Switched Capacitor Filter

2.6 Latched Comparators

A comparator is used to compare two voltages and determine which one is larger. A simplistic approach for realizing a comparator is to use an open-loop operational amplifier, as shown in Figure 2.21.[5] The illustration shows that when the voltage on the non-inverting side of the comparator is greater than the inverting side, the output of the comparator is high (or positive). Likewise, if the voltage on the inverting side of the comparator is greater than the non-inverting side, the output of the comparator is low.

In the case of delta modulation, a latched comparator is used to replace a continuous time signal with a staircase approximation[2]. The addition of a latch limits the rail-to-rail output of comparator so that the comparator can switch more quickly.

Each of the proposed designs for the latched comparator was drawn and later simulated using the simulation tool. Circuits that performed as expected were then incorporated into the schematic of the ΣΔM and tested.

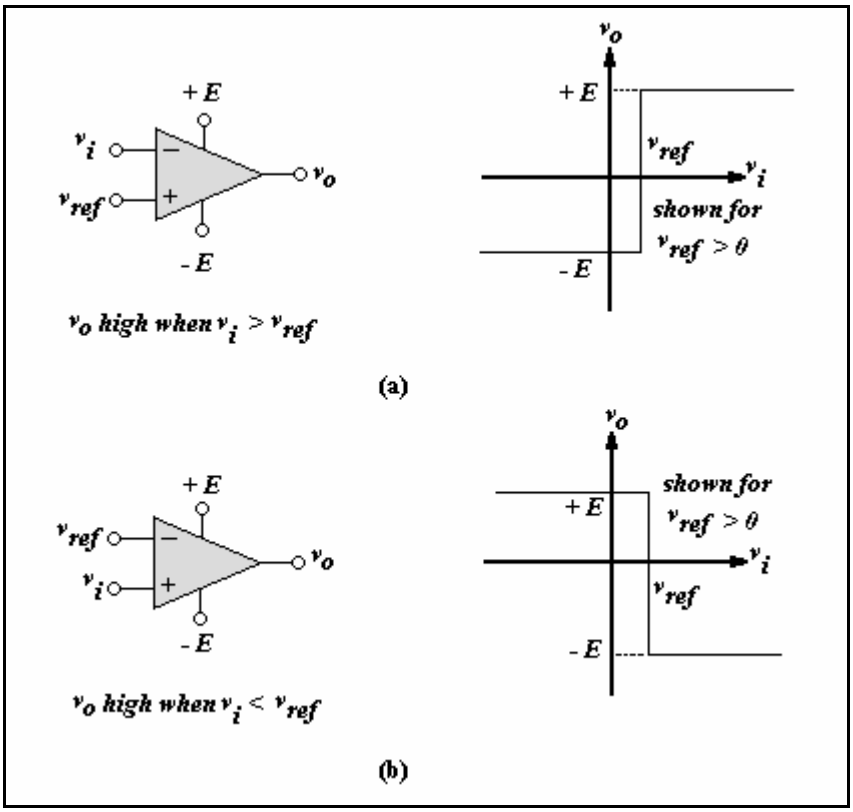

Figure 2.21: (a) Comparator Output When $v_i > V_{ref}$
(b) Comparator Output When $v_i < V_{ref}$ [5]

2.6.1 Design requirements

The simplest way to design a latched comparator is to add several latches to the output of an op-amp. As illustrated in Figure 2.22, the op-amp is used to compare two input voltages while the latch effectively limits the output swing of the amplifier.

To produce meaningful output, this configuration demands an amplifier with a fast slew rate. During its initial stages of development, this type of architecture was implemented using a folded-cascode amplifier. All switches were drawn to minimum feature size. Unfortunately, a T-Spice™ simulation demonstrated that this circuit was unable to meet the slew rate requirements of the ΣΔM. Consequently, it was necessary to design a new latched comparator that could satisfy the extraordinary requirements of analog-to-digital conversion.

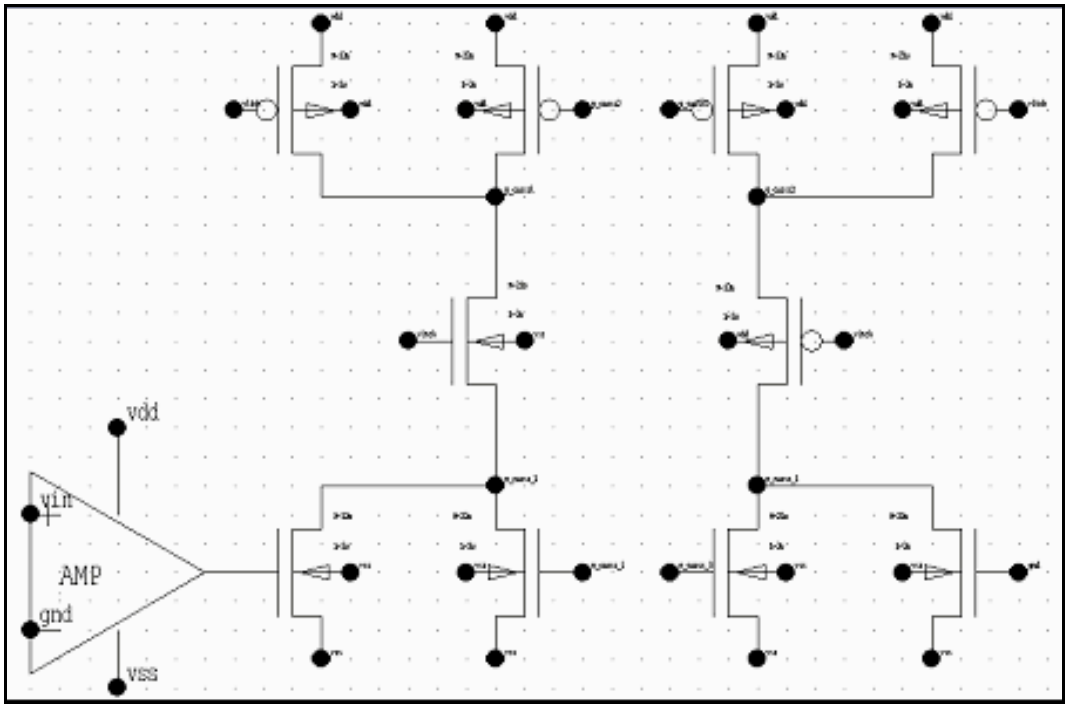

Figure 2.22: Latched Comparator Utilizing Op-amp

As shown in Figure 2.23, the new architecture proposed by Song was able to meet the slew rate requirements necessary for the circuit.[12] This architecture consists of four basic stages. The first stage of the latched comparator is the circuit bias stage. A single PMOS transistor controls all the current that flows through the entire circuit. In addition, this transistor isolates the circuit from power supply noises. The current from the drain of the PMOS flows to the source and gate of an NMOS device where it is mirrored to the second stage of the circuit. The second stage of the amplifier functions as a preamplifier. The diode connected loads of the preamplifier stage provide a limited amount of gain to maximize speed.

The third stage of the circuit is the gain stage. During the track and latch stage when the two diode connected transistors are enabled, the gain around the positive feedback loop of stage four is less than one and the circuit is sTable. [12]

As seen in Figure 2.23, input signals are applied to the left and right side of the difference mode amplifier that makes up the preamp stage. The output of the comparator is taken from each side of the positive feedback loop.

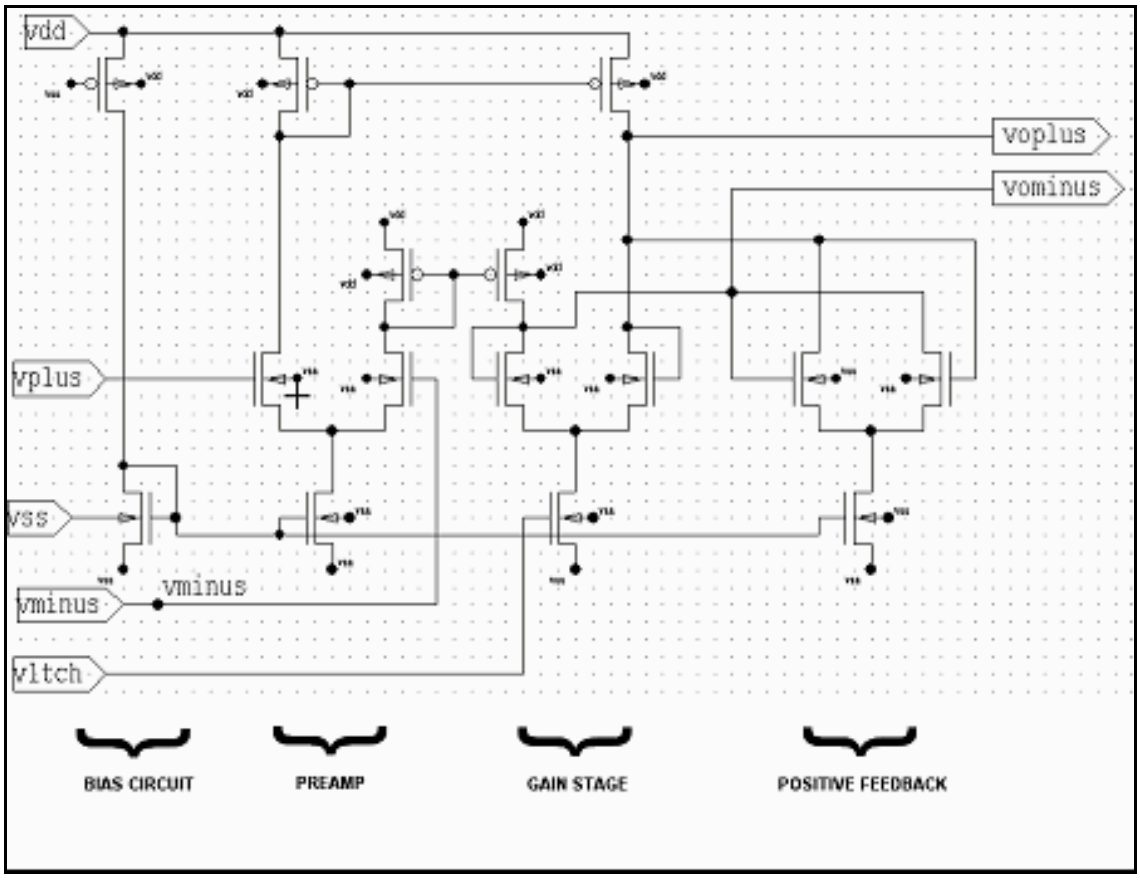

Figure 2.23: Song Latched Comparator

2.6.2 Morphed schematic of the latched comparator

Many of the transistor modules from the folded-cascode amplifier were used to build the latched comparator. In most instances, only half of a given transistor pair was used in the design. Ultimately, this approach did not lead to an effective use of space; however, it did greatly speed up the layout process. The morphed schematic of the latched comparator is illustrated in Figure 2.24.

With the exception of the PMOS bias transistor, each transistor is uniquely identified by a letter and number. A corresponding letter and number has also been assigned to each transistor pair in the circuit layout. An "R" or "L" indicates that a transistor is located in the right or left hand column of transistors in the layout. The number assigned to each transistor distinctly identifies the row location of each transistor

in the layout. This approach allows each transistor pair to be identified quickly and routed.

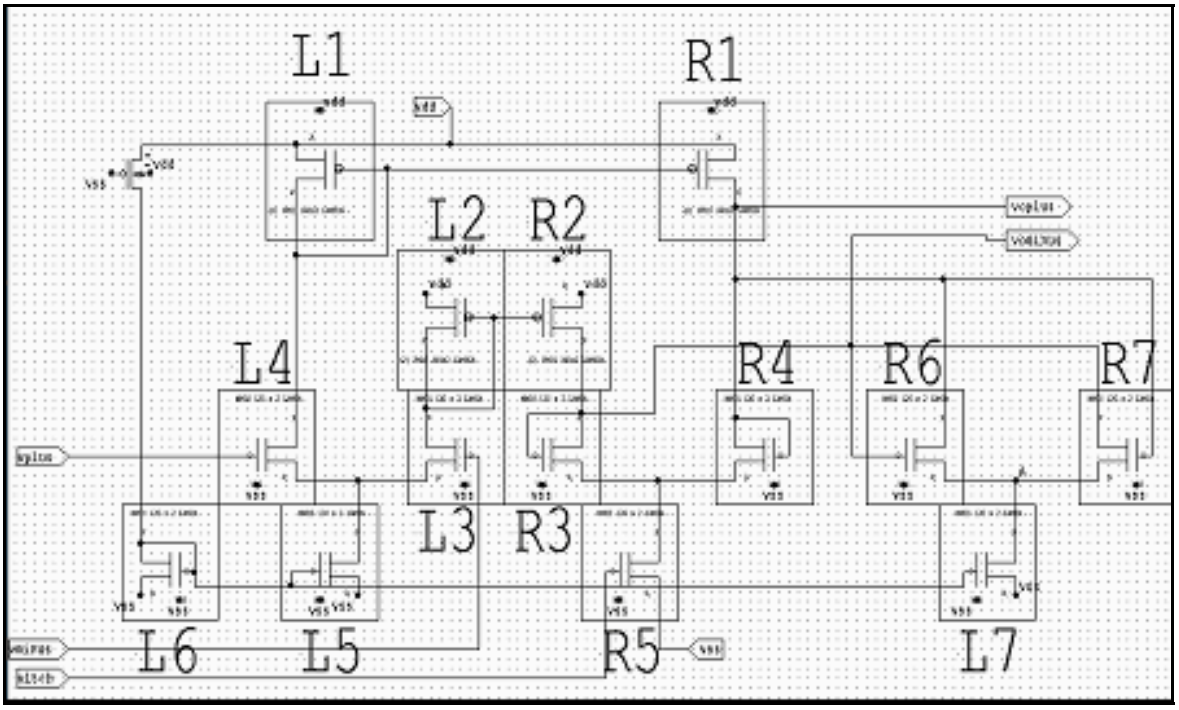

Figure 2.24: Morphed Schematic of the Latched Comparator

With the exception of the bias PMOS, identical aspect ratios were used for all NMOS and all PMOS devices. Table (IV) lists the transistor aspect ratios for the latched comparator.

Table IV: Latched Comparator Aspect Ratios

Transistor	L1	L2	L3	L4	L5	L6	L7	
Aspect ratio (W/L in um's)	360/2	360/2	120/2	120/2	120/2	120/2	120/2	

Transistor	R1	R2	R3	R4	R5	R6	R7	BIAS
Aspect ratio (W/L in um's)	360/2	360/2	120/2	120/2	120/2	120/2	120/2	30/2

2.6.3 Layout of the latched comparator

As shown in Figure 2.25, the layout of the latched comparator was divided into two columns ands seven rows. Each row (1-7) and column (R, L) uniquely identify a transistor pair in the circuit schematic.

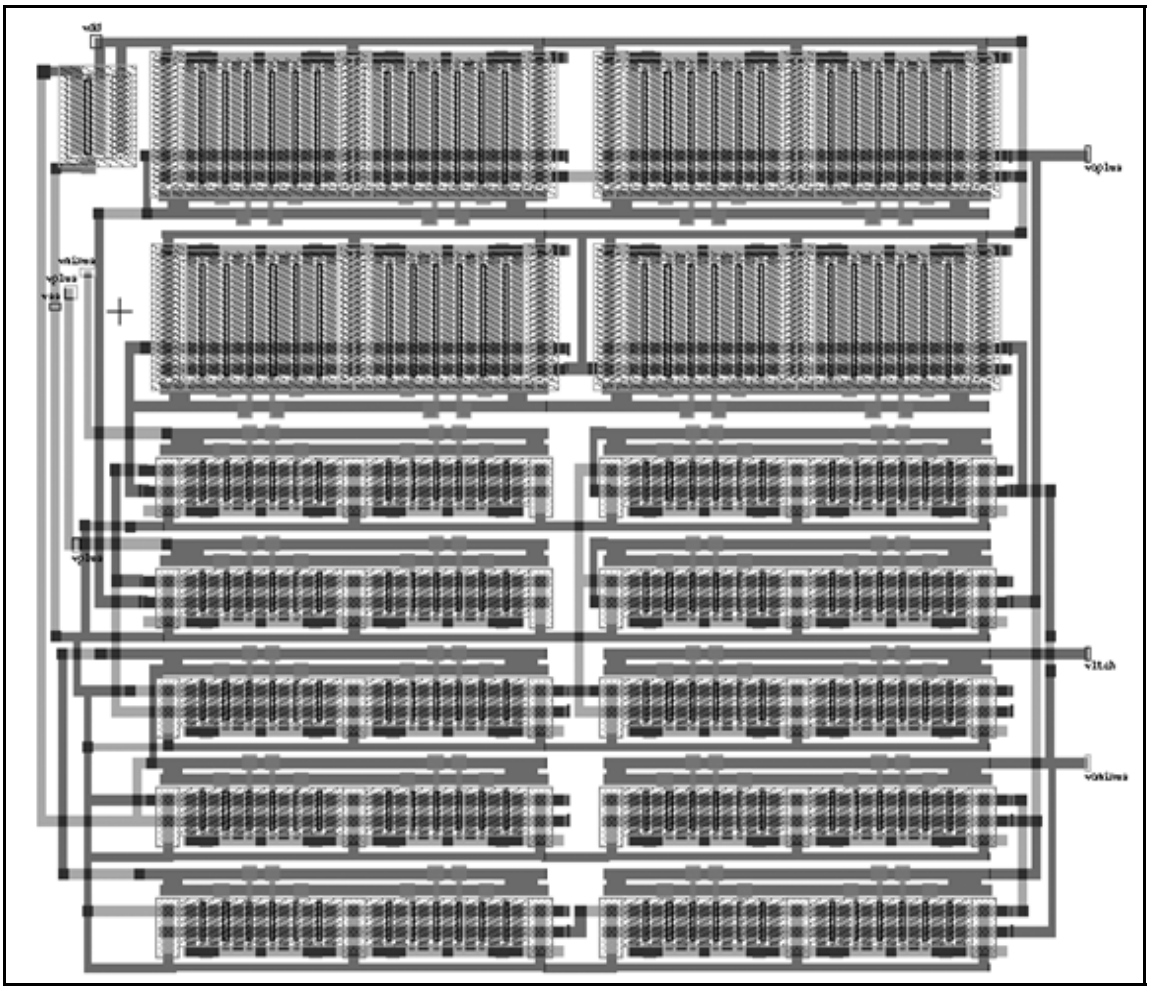

Figure 2.25: Layout of the Latched Comparator

Due to its exact size requirement, the bias PMOS transistor was drawn from scratch. In most instances, a scaled NMOS or PMOS pair from the folded-cascode amplifier layout was used in the layout of the latched comparator. This design technique greatly reduces the amount of time spent drawing transistor pairs. Common input signals were connected together to minimize the amount of pads required for the design.

2.7 D/A Converter

The primary function of the D/A (digital-to-analog converter) is to provide feedback for the modulator. Basically, the D/A converts the digital output of the modulator back to an analog, continuous signal. The converted signal is then fed back into the inputs of the modulator.

2.7.1 Design requirements

The D/A was created by modifying the schematic of the latched comparator. The schematic of the D/A is shown in Figure 2.26.

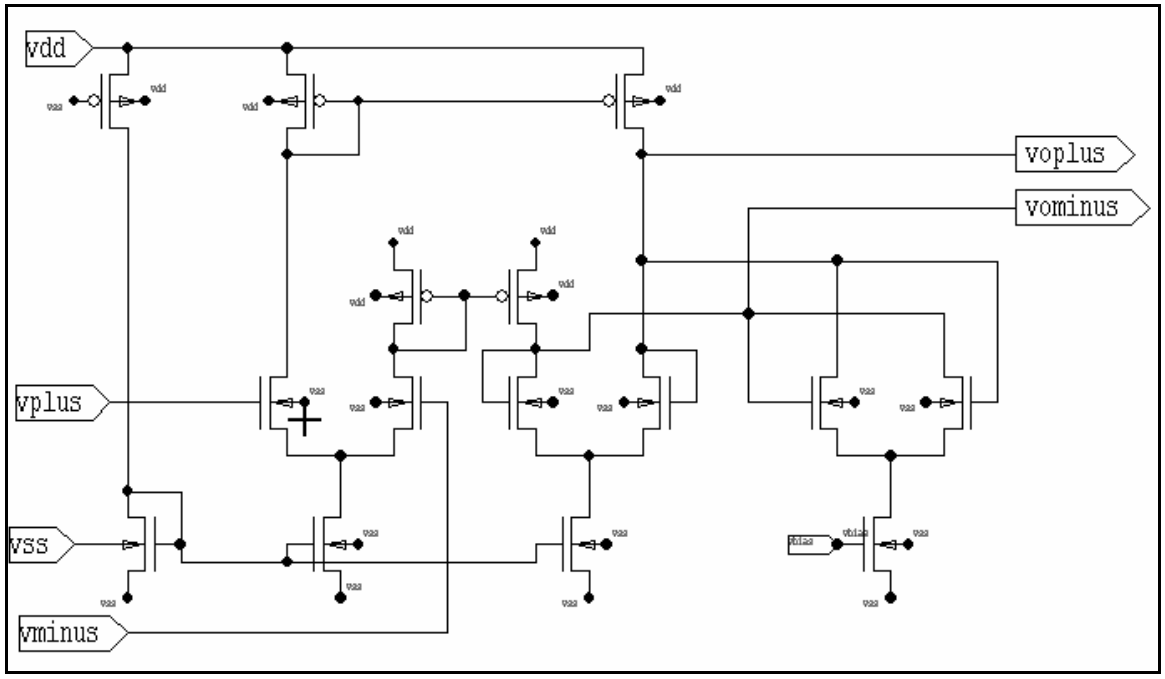

Figure 2.26: Schematic of the D/A

As illustrated in Figure 2.26, the signal "VLTCH" of the latched comparator was rerouted to VSS. In addition, a bias voltage (vbias) was added to the positive feedback loop. The amount of positive feedback can be varied by changing vbias.

The operation of the D/A is similar to the operation of the latched comparator. When the voltage on the non-inverting side of the D/A is greater than the inverting side, the output of the D/A is high (or positive). Likewise, if the voltage applied to the non-inverting input is less than the inverting input, the output of the D/A is low. However, unlike the latched comparator, the slew rate of the circuit is not controlled by a latch. Moreover, the additional bias control on the circuit feedback loop can be used to scale the output.

2.7.2 Morphed schematic of the D/A

The morphed schematic of the D/A was easily created by modifying the morphed schematic of the latched comparator. As illustrated in Figure 2.27, an additional bias voltage (vbias) was added to the feedback loop of the circuit. The tail of the difference mode amplifier which was previously controlled by the signal "VLTCH" was connected to VSS.

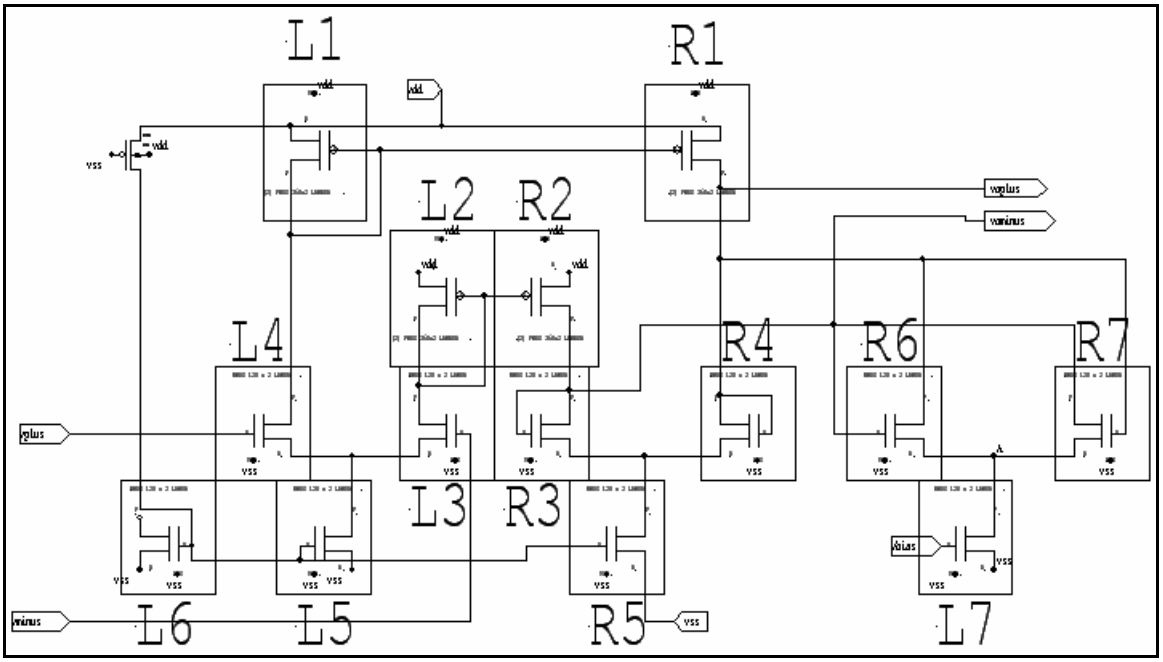

Figure 2.27: Morphed Schematic of the D/A

A schematic-entry approach similar to the approach used for the latched comparator was used for the D/A. As shown in Figure 2.27, each transistor of the D/A circuit has been assigned an alphanumeric code. Each code uniquely identifies that position of the transistor in the circuit layout. The layout of the D/A was divided into two columns of transistors, each containing seven transistors (seven rows). An "R" or "L" designation identifies if a transistor is located in the right or left column of the layout. The number immediately following the column designation uniquely identifies the row position of each transistor. This layout and schematic-entry approach allows the transistors in the circuit to be quickly and more precisely wired. Also, in the event that the circuit does not pass a layout-versus-schematic test, the unique identification of transistors allows problems to be found more quickly.

A set of transistor aspect ratios that are identical to the latched comparator were used for the layout of the D/A. The D/A aspect ratios are shown in Table (V).

Table V: D/A Transistor Aspect Ratios

Transistor	L1	L2	L3	L4	L5	L6	L7	
Aspect ratio (W/L in um's)	360/2	360/2	120/2	120/2	120/2	120/2	120/2	

Transistor	R1	R2	R3	R4	R5	R6	R7	BIAS
Aspect ratio (W/L in um's)	360/2	360/2	120/2	120/2	120/2	120/2	120/2	30/2

2.7.3 Layout of the D/A

The layout of the D/A was completed by copying the layout of the latched comparator and making a few subtle modifications. As shown in Figure 2.28, the node "VLTCH" was reconnected to VSS. Additionally, the gate of the transistor on the tail of the feedback loop was wired to an isolated pad. The remainder of the layout was left unchanged.

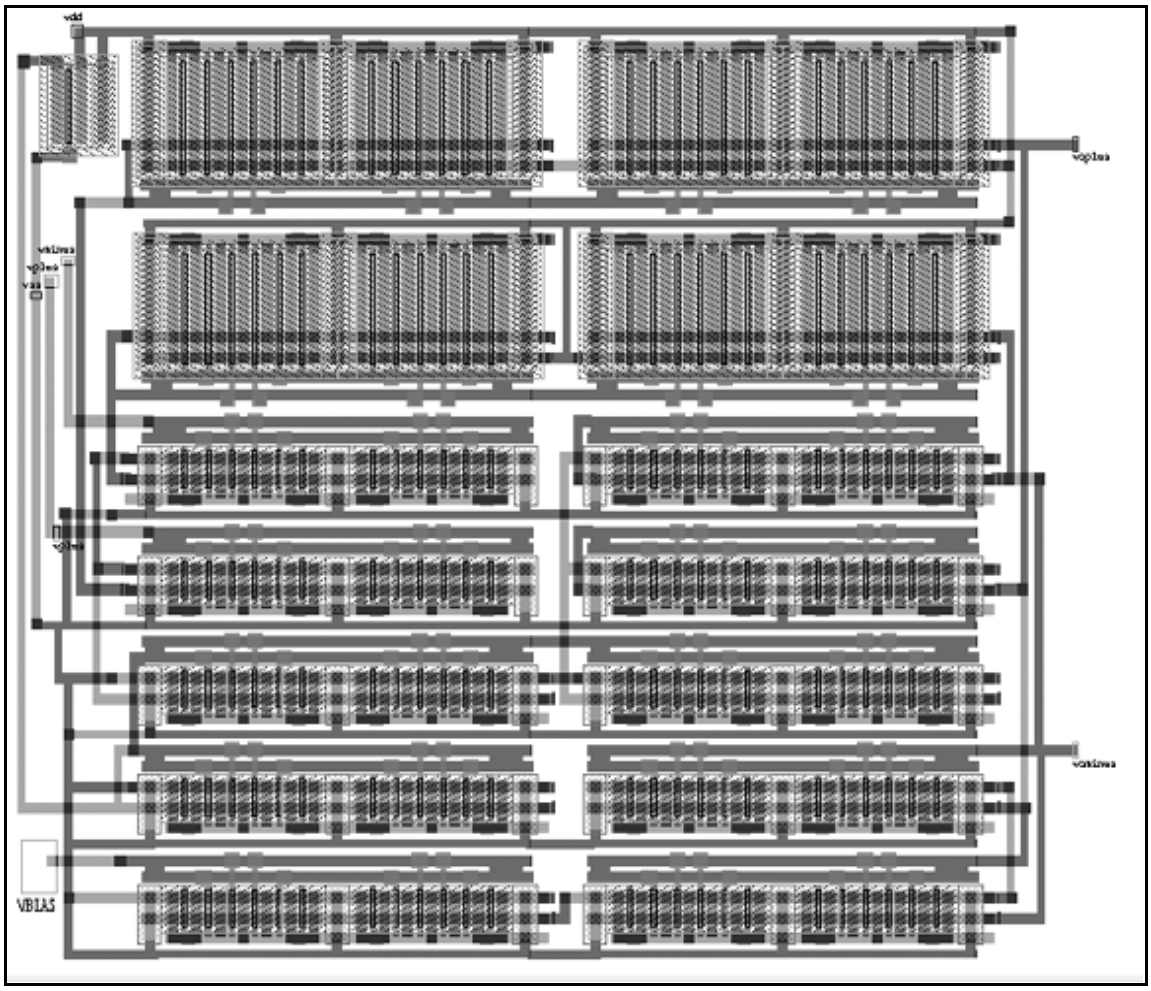

Figure 2.28: Layout of the D/A

2.8 ΣΔM

To conclude this work, the switched capacitor filter, latched comparator and D/A were all combined to form a complete ΣΔM. The completed circuit is shown in Figure 2.29.

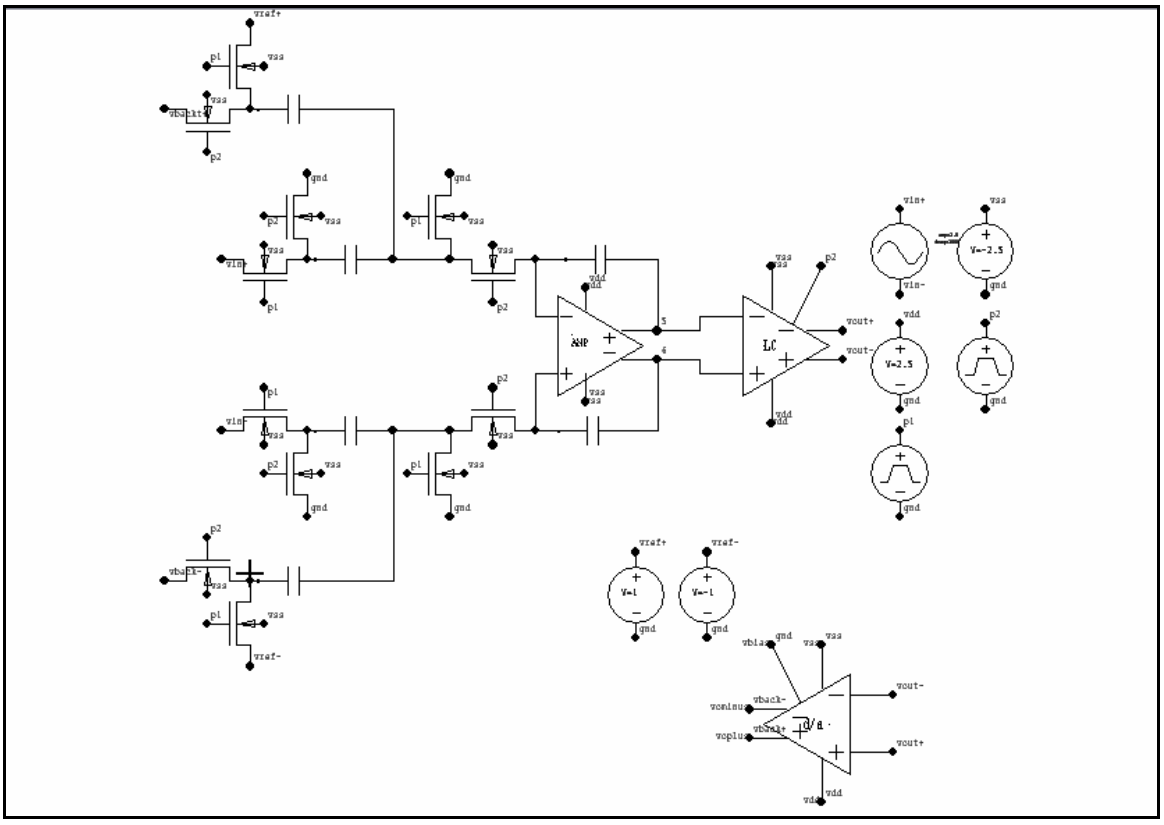

Figure 2.29: Schematic of the ΣΔM

As previously discussed, this circuit utilizes the switched capacitor filter with the switches drawn to minimum feature size. In addition, the nodes *vref*+ and *vref*- were added to each leg of the filter to allow for fine tuning of the circuit output.

The D/A appears unattached to the circuit; however it is connected to the A/D by the nodes *vout*+ and *vout*-. The output of the D/A is fed back into the legs of the switched capacitor filter through nodes *vback*+ and *vback*-.

2.8.1 Morphed schematic of the ΣΔM

The morphed schematic of the ΣΔC was assembled by combining the individual sections of the circuit. The switched capacitor filter was unchanged during the initial development of the circuit, so a morphed schematic was not required. However, each

side of the filter utilizes an identical set of transistor and capacitors. As a result, a symbol was drawn for one leg of the circuit and then instanced on the other side of the amplifier. Figure 2.30 illustrates the symbol used in the ΣΔM schematic and the new schematic of the filter.

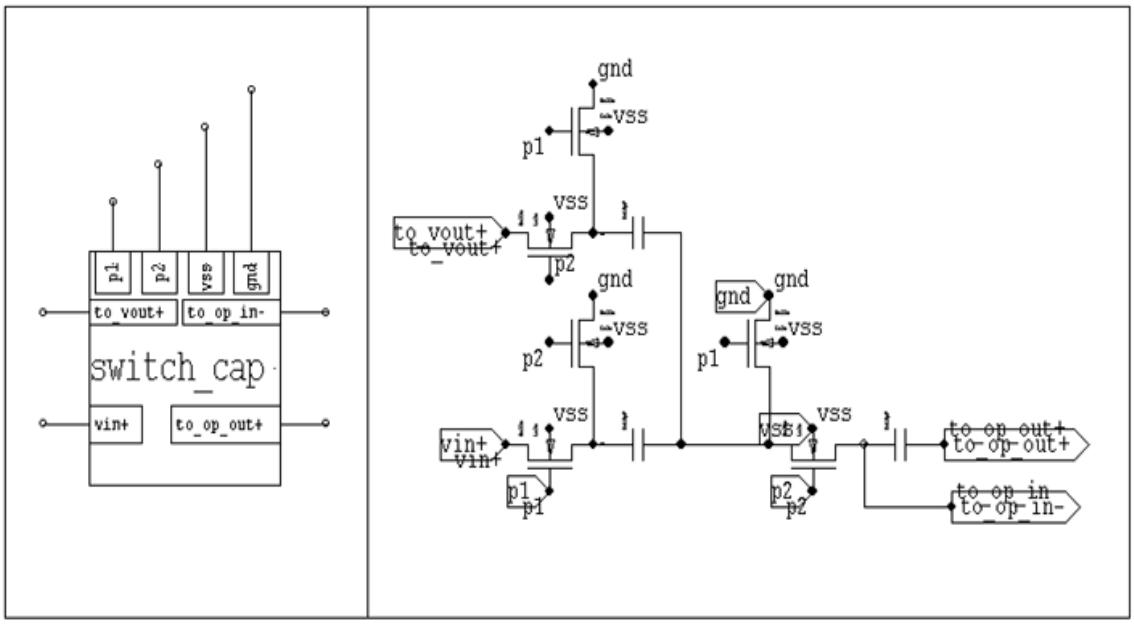

Figure 2.30: (a) Switched Capacitor Symbol
(b) Switched Capacitor Schematic

The remainder of the circuit was constructed using the following schematics:

- Morphed schematic of the latched comparator.
- Morphed schematic of the folded-cascode amplifier
- Morphed schematic of the D/A (modified version of the latched comparator schematic.

Figure 2.31 illustrates the complete morphed schematic of the ΣΔM.

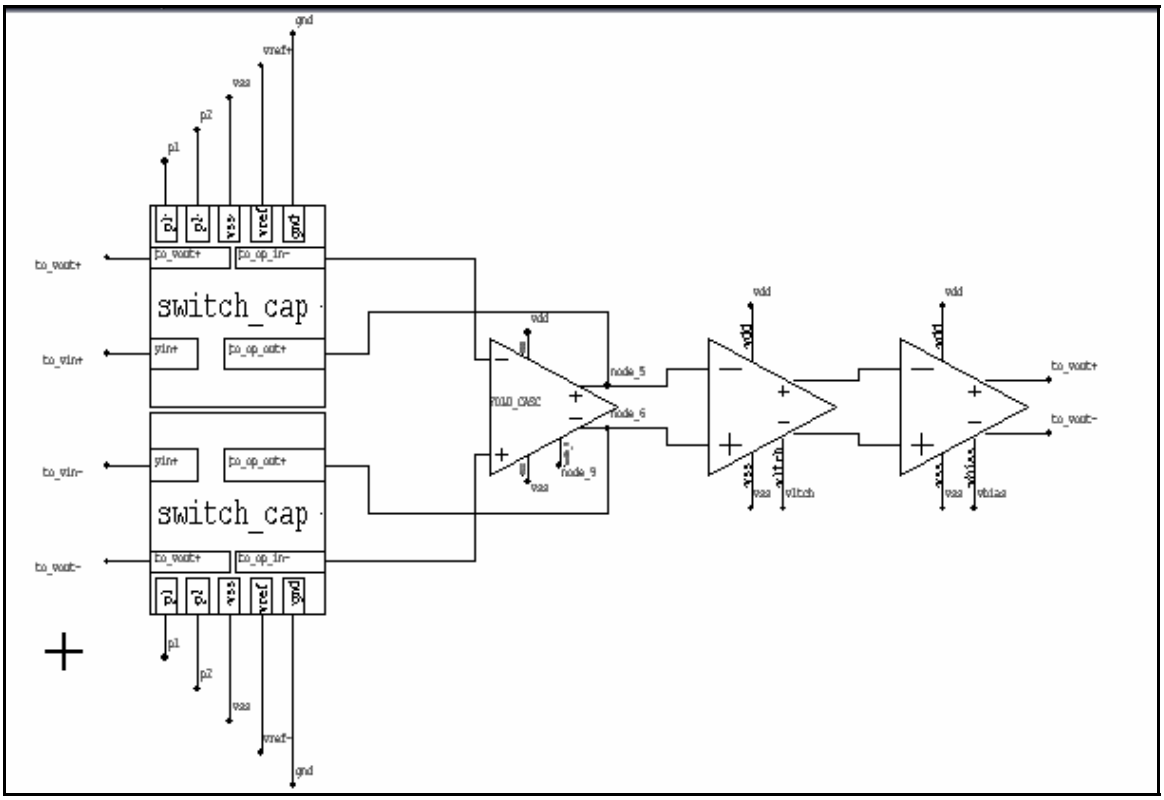

Figure 2.31: Morphed Schematic of the ΣΔM

2.8.2 Layout of the ΣΔM

The layout of the complete modulator was assembled by wiring together the layout of each individual part. The modulator was created using the following layouts:

- Scaled layout of the folded-cascode op-amp.
- New layout of the latched comparator.
- New layout of the D/A.
- New layout of the switched capacitor circuit.

The modulator utilizes the smaller version of the switched capacitor circuit with the switches drawn to minimum feature size. The completed modulator is illustrated in Figure 2.32.

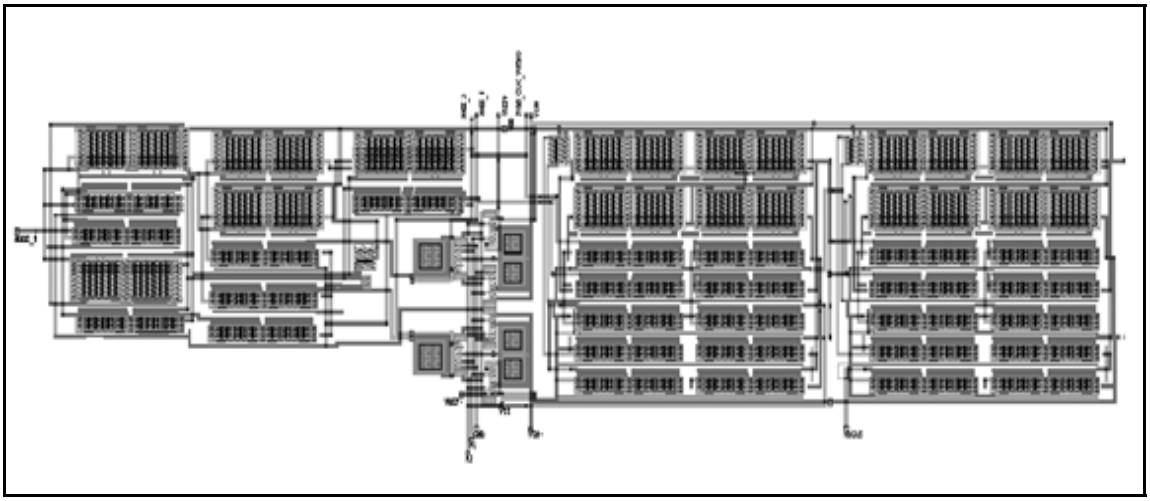

Figure 2.32: Complete Layout of the ΣΔM

In general, the individual parts of the ΣΔM were grouped together as tightly as possible to minimize wasted space. In an effort to keep a neat appearance and reduce the number of unnecessary wires, common signals were connected together and then a single wire was used to connect them to a pad. The completed circuit measures approximately 1715 lambda in length (left to right) and is 432 lambda in height (top to bottom),

3. RESULTS AND ANALYSIS

3.1 Folded Cascode Amplifier

The design of the folded-cascode operational amplifier was crucial for the proper operation of the analog-to-digital converter. In addition to providing most of the required gain for the circuit, the op-amp was also one of the major limiting factors of the analog-to-digital converter's slew rate. The amplifier was simulated using the 1.6um parameters and 0.5um parameters to ensure that the circuit achieved a comparable gain. Each simulation was performed using the following approach:

- -2.5V to 2.5V split supply.
- Non-inverting side of amplifier connected to ground.
- Inverting side driven by sine wave input.
- DC operating point calculation.

A standard AC analysis was used to determine the approximate gain and phase of the amplifier. The commands used to perform an AC analysis are shown below:

.options accurate
.ac dec 3 100 1e8

Due to a discrepancy between version 7 and version 9 of T-Spice™, the first statement is used to ensure that the different versions of the simulation tool produce similar results. Without this command, different versions of the simulation tool will calculate the DC operating point of the amplifier using different techniques and produce very dissimilar results. The second command instructs the simulation tool to perform an AC analysis from 100Hz. to 100MHz. taking three points per decade. After the AC analysis has been executed, a "print" statement can be used to display the simulation results:

.print ac vp(out+) vdb(out+)

This statement instructs the simulation to plot the results of the simulation for the non-inverting output of the amplifier, “out+”.

Figure 3.1 illustrates the output of the folded-cascode amplifier using 1.6um process parameters.

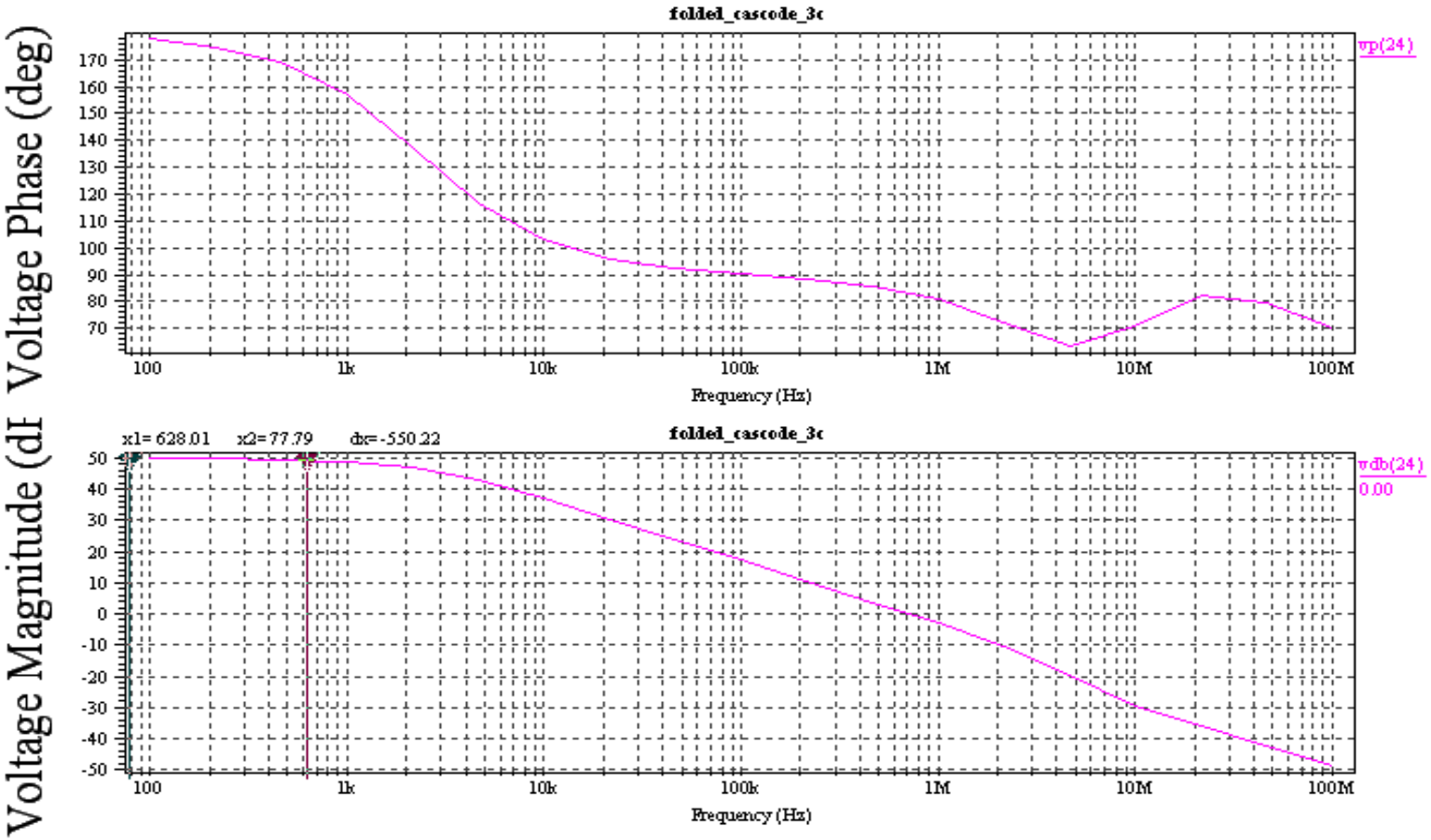

Figure 3.1: Folded Cascode Output Using 1.6um Parameters

As shown, the amplifier was able to achieve a voltage gain of nearly 50 db. However, the amplifier has a fairly narrow bandwidth. From inspection, the -3dB point of the amplifier is approximately 2.27KHz. The unity gain bandwidth of the amplifier is approximately 700KHz.

In addition to the 1.6um process simulation, the amplifier was also simulated using 0.5um parameters. However, the amplifier performed poorly when using the aspect ratios from the 1.6um process. Consequently, an updated schematic that was originally intended for use in a 0.7um process was used for the simulation. The simulation results are shown in Figure 3.2.

As Figure 3.2 illustrates, the amplifier was able to achieve more gain. This can be attributed to the change in the gate capacitance C_{OX}. This behavior can be explained by a closer inspection of the square law model. As the gate-oxide capacitance is increased, the amount of current allowed to flow through the drain of the transistors also increases. The increased current allows the amplifier to achieve more gain.

From inspection, the -3db point of amplifier occurred near 4.04KHz at a gain of 60.55db. The unity gain bandwidth of the updated design is approximately 10MHz. This is a noticeable improvement over the unity gain bandwidth of the amplifier simulated with the 1.6um parameters. In addition, the amplifier consumed 0.54 mW of power.

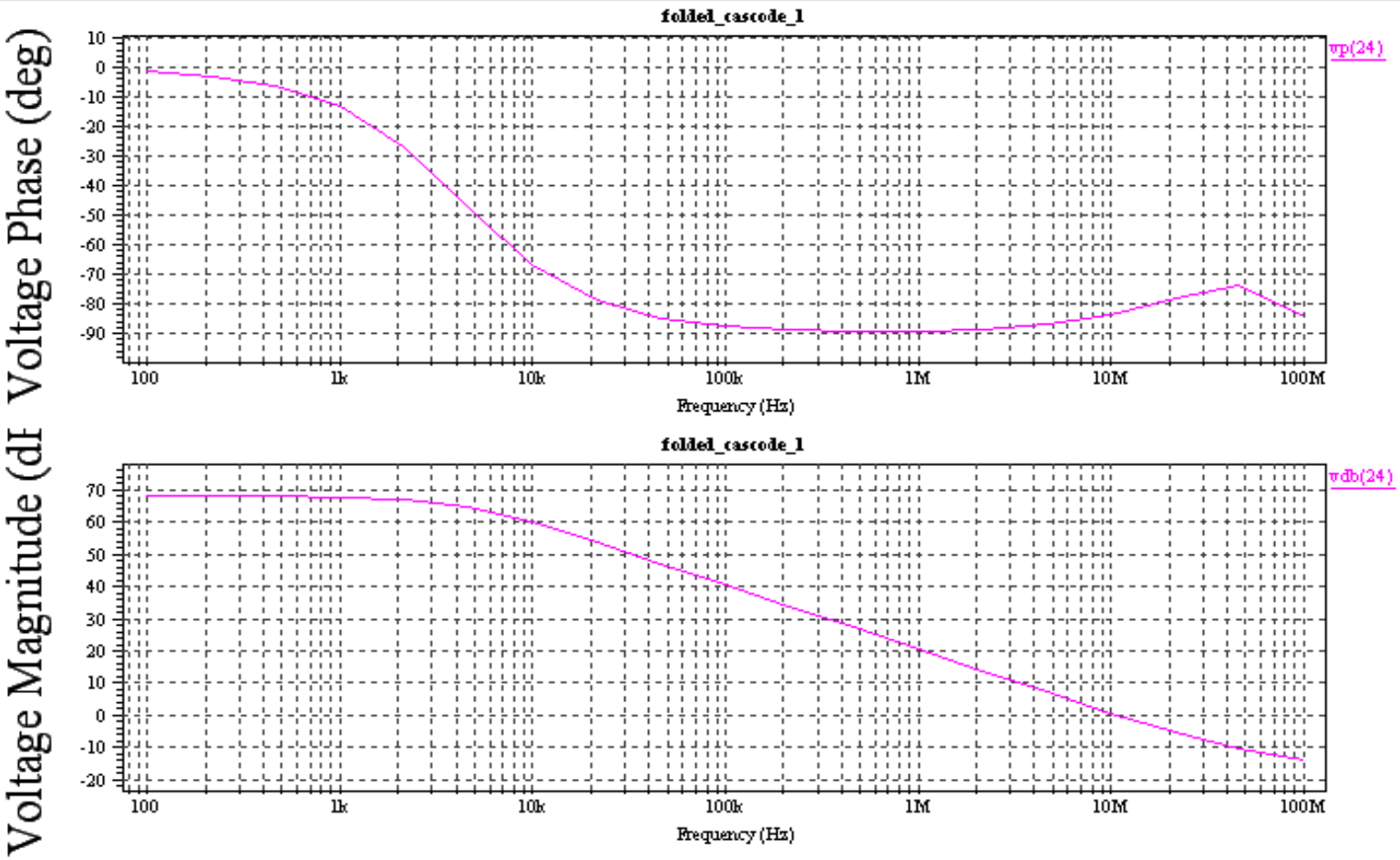

Figure 3.2: Folded-Cascode Output Using 0.5um Parameters

3.2 Switched Capacitor Filter

The folded-cascode operational amplifier was used for all switched capacitor simulations. The switches of the circuit were all drawn to minimum feature size to achieve the maximum switch rate. To simplify the simulation of the switched capacitor filter, the circuit was reduced to a single sided, single output filter. The unused side of the amplifier was connected to ground. Figure 3.3 illustrates the switched capacitor filter that was used in the simulations

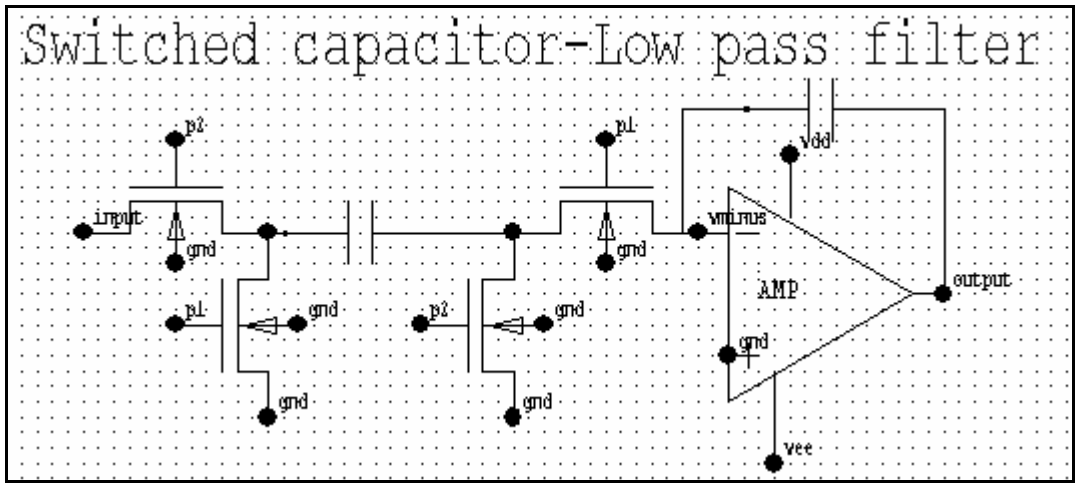

Figure 3.3: Switched Capacitor Filter (Simulation)

Like the other parts of the ΣΔM, the switched capacitor filter was simulated using the 1.6um and 0.5um parameters obtained from the MOSIS Service. Each simulation was performed using similar characteristics and approaches:

- -2.5V to 2.5V split supply.
- Non-inverting side of amplifier connected to ground.
- Inverting side driven by sine wave input.
- Pulse (square wave) input applied to switches.
- DC operating point calculation.
- Transient analysis combined with frequency sweep.

The pulses used to drive the switching circuitry are shown in Figure 3.4.

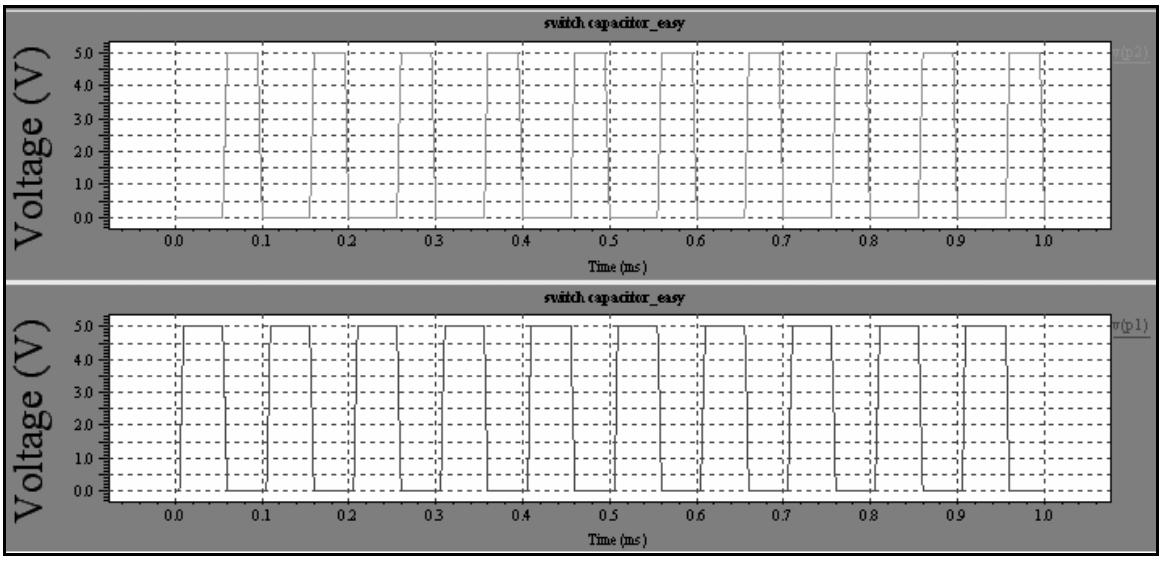

Figure 3.4: Pulses Used to Drive Switched Capacitor Switching Circuitry

As Figure 3.4 illustrates, the pulses used to drive the switches are identical in amplitude and shape, however, they are completely out of phase with one another.

A less orthodox transient analysis method was used to simulate the switched capacitor filter. A transient analysis (or time-domain analysis) can be used to find the response of the circuit to initial conditions and time-dependent stimuli. This type of analysis was used to observe the output of the filter at various frequencies. The basic commands used to perform the transient analysis are shown below:

.param freq=100
.tran/op 1e-2 .01 method=bdf sweep dec param freq 100 10000 2

The first command defines a variable (***freq***) and initializes it to 100Hz. The second instruction is the actual transient analysis simulation command. This command instructs the simulation tool to perform a transient analysis for the variable ***freq*** from 100Hz. to 1000Hz. taking two points per decade. The "/op" command instructs the simulation tool to perform a DC operating calculation before simulation to determine initial steady-state node voltages. The addition of "method=bdf" commands the simulation tool to use Gear's backward differentiation method of calculation for the

transient analysis. In this method, the time derivative of charge in the KCL Equation is replaced by an approximation involving the solution at the last few time points. Once a simulation has been executed, the print statement shown below can be used to display the simulation results:

.print tran v(output)

This command instructs the simulation tool to display the output (voltage magnitude) at the output node of the circuit. Figure 3.5 illustrates the results of the transient analysis. As illustrated, a curve was generated for each frequency of the input sweep. The response of the filter was determined by observing the peak-to-peak output voltage of the circuit at different frequencies. The bottom chart of Figure 3.5 shows that as the frequency is increased, the amplitude of the output signal (peak-to-peak) decreases. This trend suggests that the circuit is blocking higher frequencies and does indeed operate as intended. The cutoff point of the filter is approximately 1000Hz at 1.43V.

An identical filter was also simulated using the AMI 0.5um process parameters. The results of the 0.5um simulation are shown in Figure 3.6. As illustrated, the 0.5um parameters produced output very similar to the 1.6um process parameters. In this case, the cutoff point of filter appears to also be around 100Hz at 1.46V. However, the simulation shows that this filter has a greater offset (approximately 0.03V difference) than the filter that was simulated with 1.6um parameters.

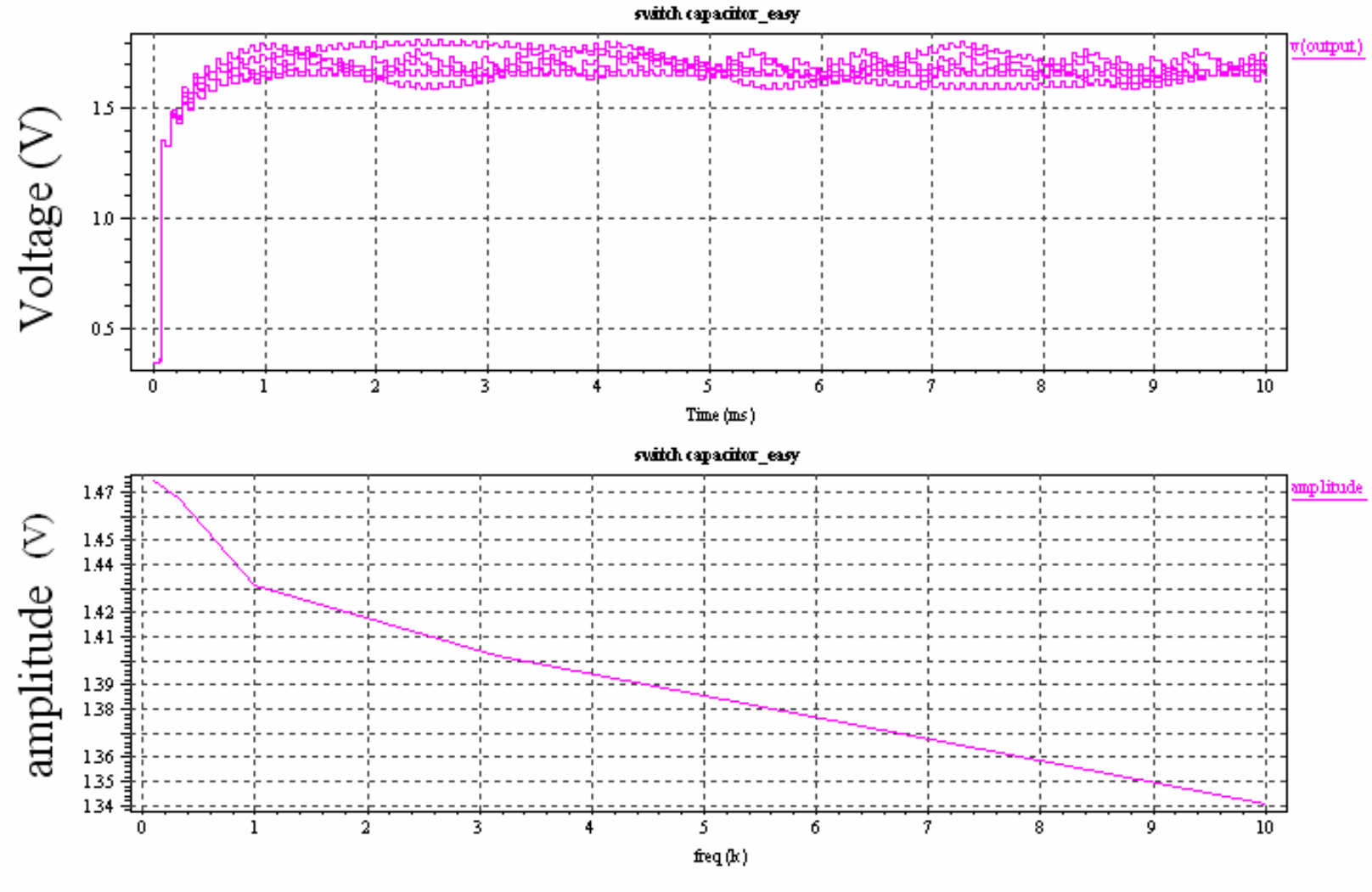

Figure 3.5: Switched Capacitor Output Using 1.6um Parameters

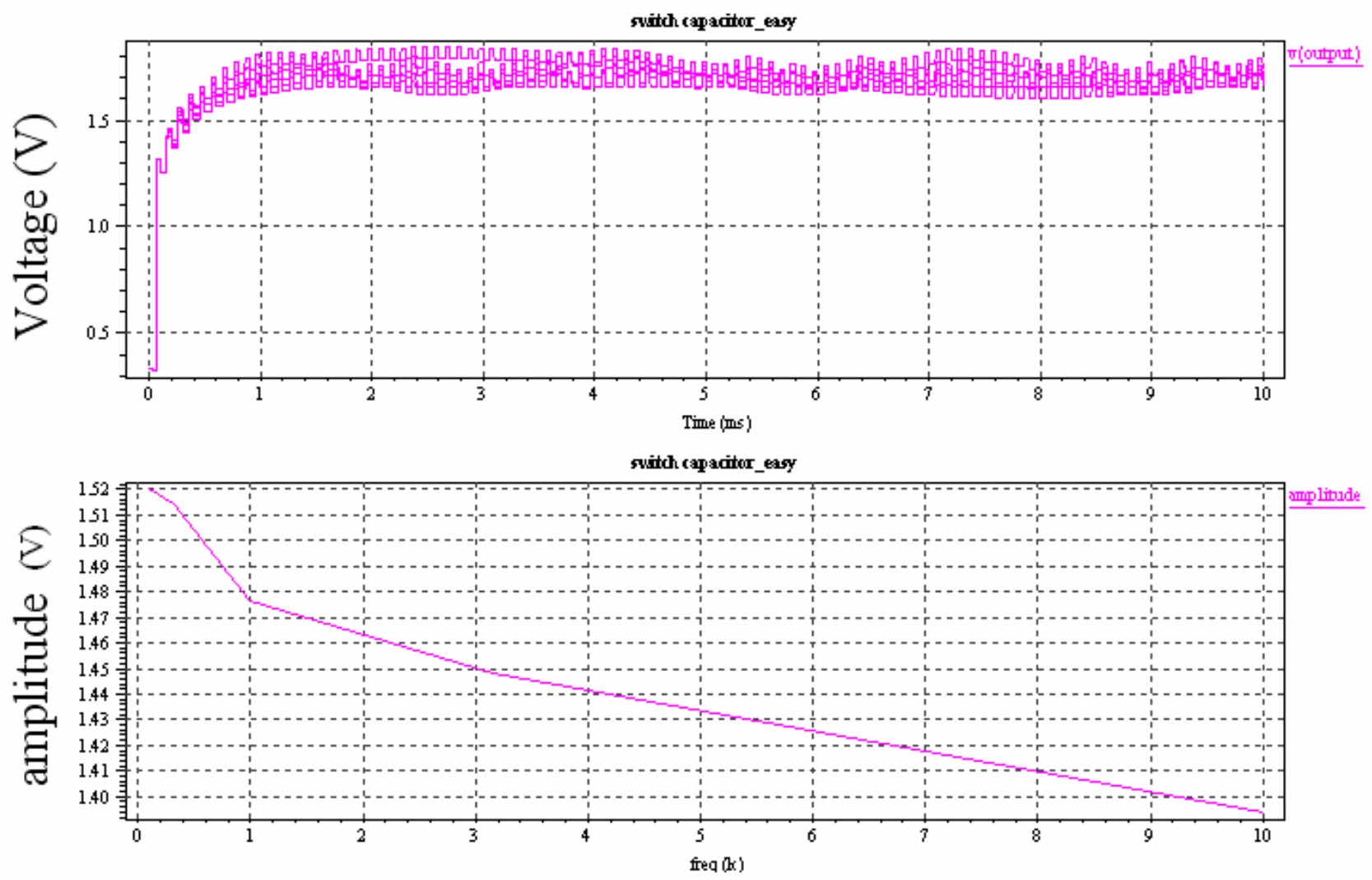

Figure 3.6: Switched Capacitor Output Using 0.5um Parameters

3.3 Simulation of the Latched Comparator

To simplify the aspect ratio calculation of the latched comparator, aspect ratios from the folded-cascode amplifier were used for a majority of circuit. However, the aspect ratio of the current-controlling PMOS of the bias stage is critical because it controls the amount of current that flows through the entire circuit. This aspect ratio was determined experimentally, by simulation.

The latched comparator was simulated using two different processes. The first simulation uses the 1.6um parameters that were used in past designs. The second simulation was performed using newer, 0.5um parameters. In each case, the parameters were obtained on-line from MOSIS's AMI runs.

Both simulations were performed using similar characteristics and approaches:

- -2.5V to 2.5V split supply.
- Inverting side of comparator connected to ground.
- Non-inverting side driven by sine wave input.
- Pulse input applied to latch circuitry.
- DC operating point calculation.
- Transient analysis.

Prior to each transient analysis, T-Spice™ was used to find the DC operating point of the circuit. A circuit's DC operating point is its steady-state, which would be reached after an infinite amount of time if all inputs were held constant. If T-Spice™ fails to find a DC operating point, then the simulation results are most likely inaccurate or may not be defined.

The circuit simulation tool sometimes uses a technique called "source stepping" to find a circuit's DC operating point. This technique gradually increases the value of each current or voltage source from zero to its final value. If it exists, The DC operating point of any circuit can be found by adding the ".op" command to a SPICE deck.

Once a DC operating point has been found, a transient analysis (or time-domain analysis) can be used to find the response of the circuit to initial conditions and time-

dependent stimuli. For the purpose of this experiment, a transient analysis can be performed by adding the following command to a SPICE deck:

.tran/op 1e-5 .001 method=bdf

The "/op" command instructs the simulation tool to perform a DC operating calculation before simulation to determine initial steady-state node voltages. The first and second numbers of the statement specify the time step and duration of the analysis. The addition of "method=bdf" commands the simulation tool to use Gear's backward differentiation method of calculation for the transient analysis.

After the simulation tool has successfully performed a transient analysis, the print command can be used to display the simulation results:

.print tran v(node, reference_node)

For each technology, the output was taken from the non-inverting output with respect to the inverting output.

For simulation purposes, the transistor aspect ratios were all left at the default size (W = 2u, L = 22u). The transient analysis was performed for 1ms using 1e-5 steps. The results of the simulation are shown in Figure 3.7

The illustration shows that the latched comparator was able to nearly achieve a rail-to-rail output. In addition, the pulsed output indicates that the latches on the amplifier are effectively limiting the circuit output. The output demonstrates that the circuit operates as expected. According to the simulation, it could be expect that the output of the amplifier was low when the input is low. Likewise, the output of the amplifier should be high when the input is a high. From illustration Figure 3.7, it can be readily seen that the amplifier follows this trend.

The latched comparator was also simulated using the 0.5um parameters obtained from MOSIS's Web site. For this simulation, the transistor aspect ratios were kept at the default size (W = 2u, L = 22u). Like the 1.6um simulation, the transient analysis was

performed for 1ms using 1e-5 steps. The results of the simulation are shown in Figure 3.8

Figure 3.8 illustrates an output nearly identical to the 1.6um simulation results. As shown, the comparator was able to achieve slightly more gain but the difference is almost negligible. A probe of each differential pair of the circuit reveals that the comparator sources 1.578mA of current. A simple calculation shows that this is proportional to a very low 7.89mW power being consumed.

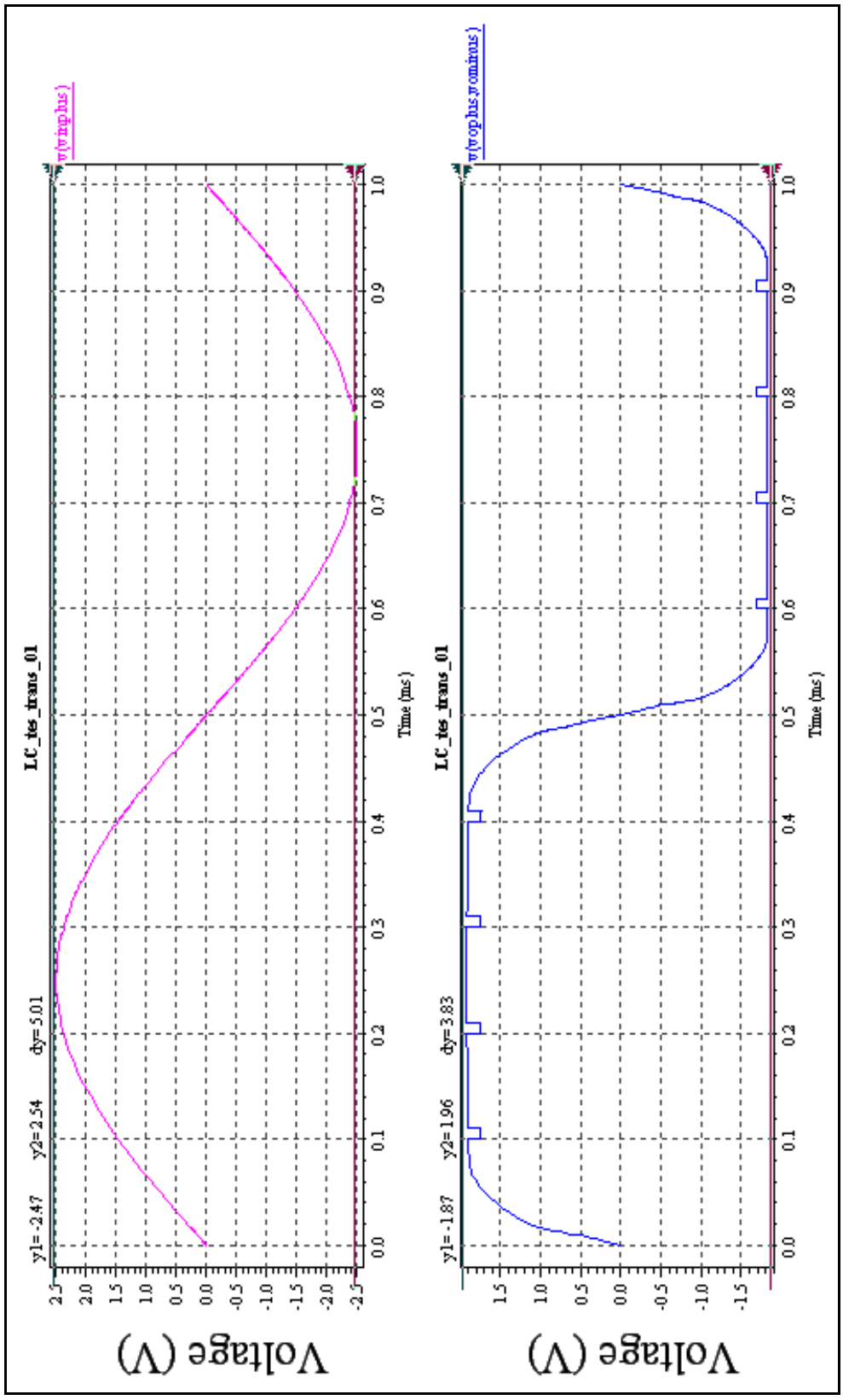

Figure 3.7: Latched Comparator Output Using 1.6um Parameters

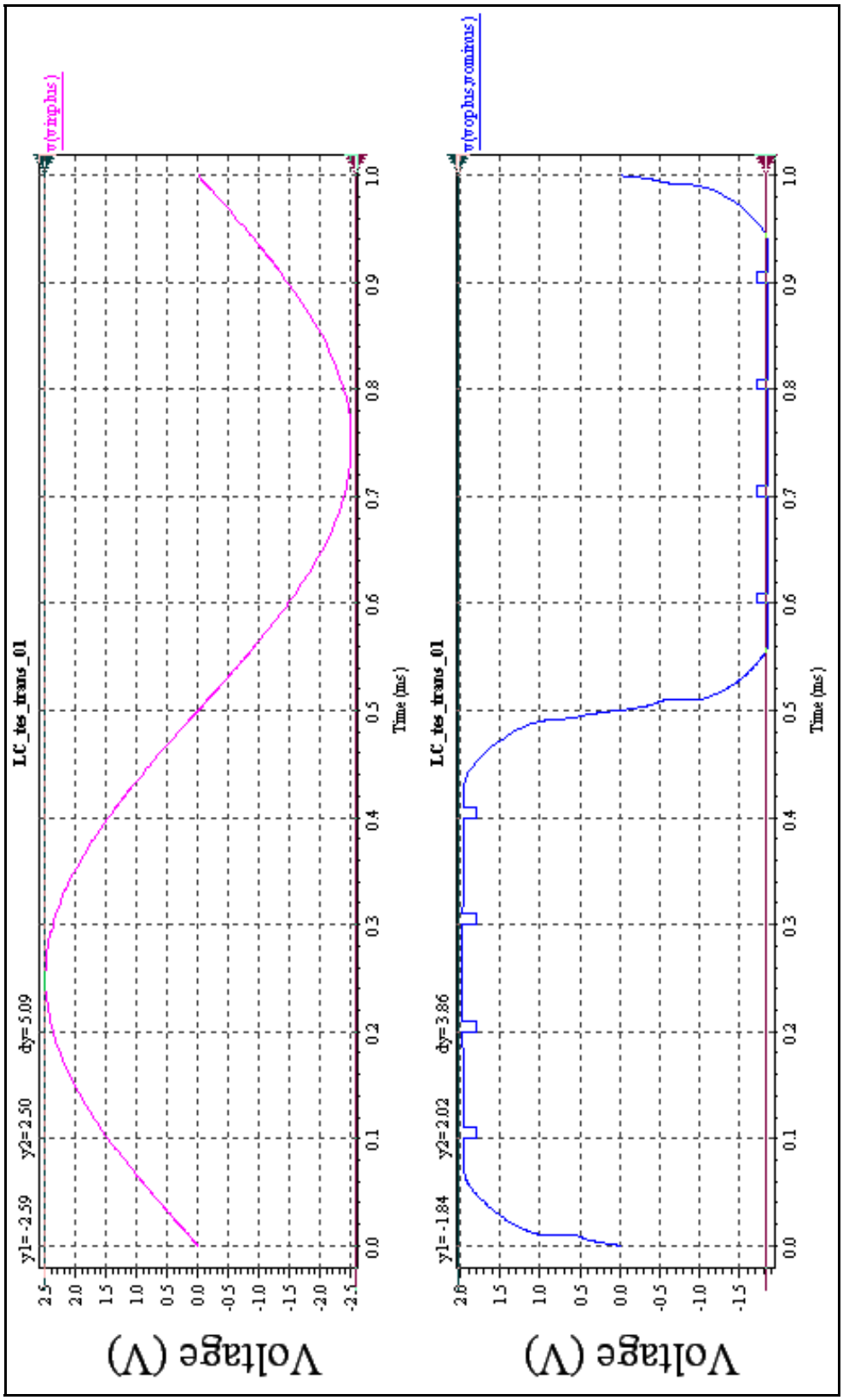

Figure 3.8: Latched Comparator Output Using 0.5um Parameters

3.4 Simulation of the D/A

The D/A is nearly identical to the latched comparator so a similar method was used to simulate the circuit. The transistor aspect ratios used in the simulation of the D/A were the same as the latched comparator. The circuit was simulated using 0.5um parameters and the approach outlined below:

Both simulations were performed using similar characteristics and approaches:

- -2.5V to 2.5V split supply.
- Inverting side of D/A connected to ground.
- Terminal "vbias" connected to ground.
- Non-inverting side driven by sine wave input.
- DC operating point calculation.
- Transient analysis.

A transient analysis that ran from 0ms to 1ms was used to determine the output of the circuit:

.tran/op 1e-5 .001 method=bdf
.print tran v(voplus)

The output of the circuit (voltage magnitude) was taken from non-inverting output of the D/A, "voplus." The print command does not specify a reference node; therefore the simulation tool assumes that the output is taken with respect to ground. The output of the D/A is shown in Figure 3.9.

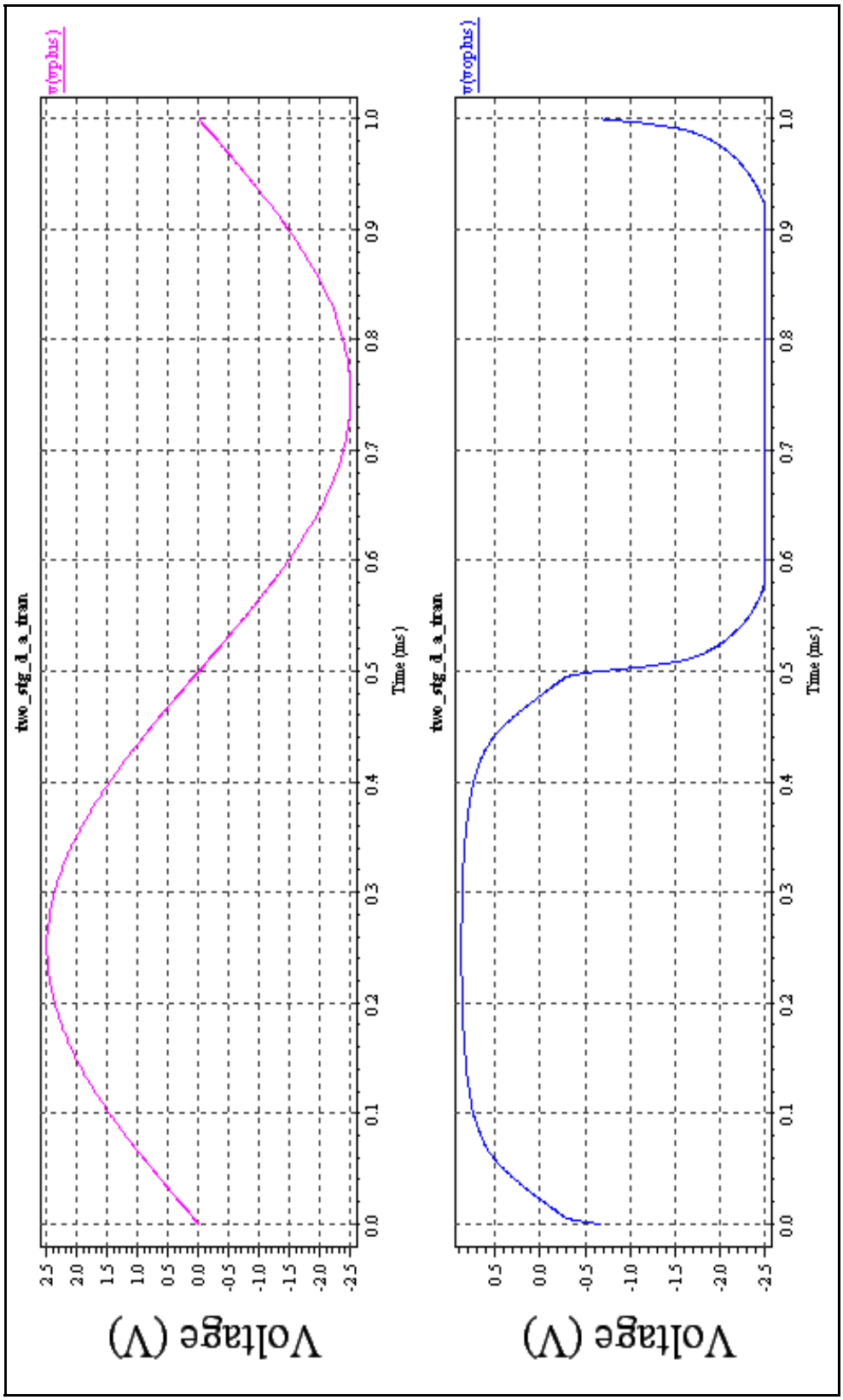

Figure 3.9: D/A Simulation Results for 0.5um Parameters

As illustrated, the circuit performs similar to the latched comparator without the "latch effect." When the voltage on the non-inverting input of the amplified was greater than ground, the output of the circuit is high. Conversely, when the voltage of the non-inverting input was below ground, the output of the D/A is low.

In addition to this simulation, a second transient analysis was used to sweep the voltage source "vbias." This simulation was used to illustrate the performance of the D/A as the amount feedback was changed. The node vbias is attached to the transistor on the tail of the feedback stage of the D/A. As vbias is changed, it is anticipated that the amount of feedback allowed to flow through the feedback loop will be reduced. Consequently, as vbias changes, the circuit will have less feedback and effectively scale the output of the D/A. The transient analysis commands used to perform this simulation are shown below:

.tran/op 1e-5 .001 sweep lin source v18 -2.5 2.5 .5

The beginning of the command ***.tran/op 1e-5 .001***, executes a standard transient analysis from 0ms to 1ms. The second half of the command instructs the simulation tool to linearly sweep the voltage source (v18) from -2.5V to +2.5V using 0.5V steps. In this example, the voltage source (v18) is directly connected to the node vbias. All other circuit parameters were identical to the previous simulation. Figure 3.10 illustrates the results of the transient analysis sweep.

As shown, the output of the D/A changes as the bias voltage is changed. However, the manipulation of vbias does not have the scaling effect that was expected. As vbias is increased from -2.5V to +2.5V the output of the D/A inverted more quickly and stays inverted for a longer period of time.

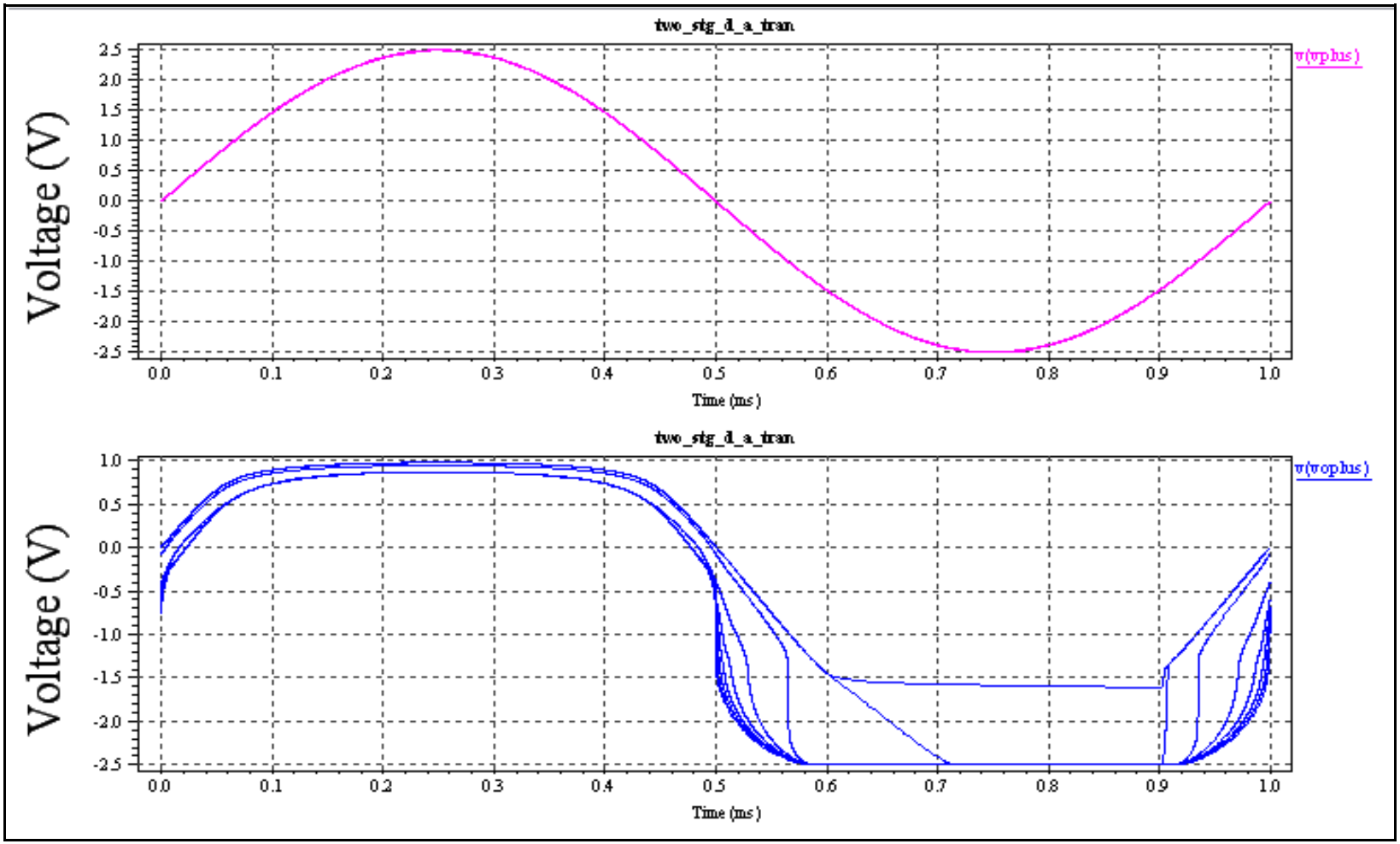

Figure 3.10: D/A Voltage Sweep Response

A probe of each differential pair of the circuit reveals that the comparator sources 11.83mA of current. A simple calculation shows that this is proportional to a very low 59.20mW power being consumed.

3.5 Simulation of the ΣΔM

The DC simulation of ΣΔM was performed under the following conditions:

- -2.5V to +2.5V split supply.
- -0.5V DC applied to inverting and non-inverting side of D/A.
- Terminal "vbias" connected to ground.
- VLTCH triggered in sync with pulse P1.
- +1VDC applied to Vref+; -1VDC connected to Vref-
- DC operating point calculation.
- Transient analysis.

The pulses *vlatch*, *p1* and *p2* are shown in Figure 3.11.

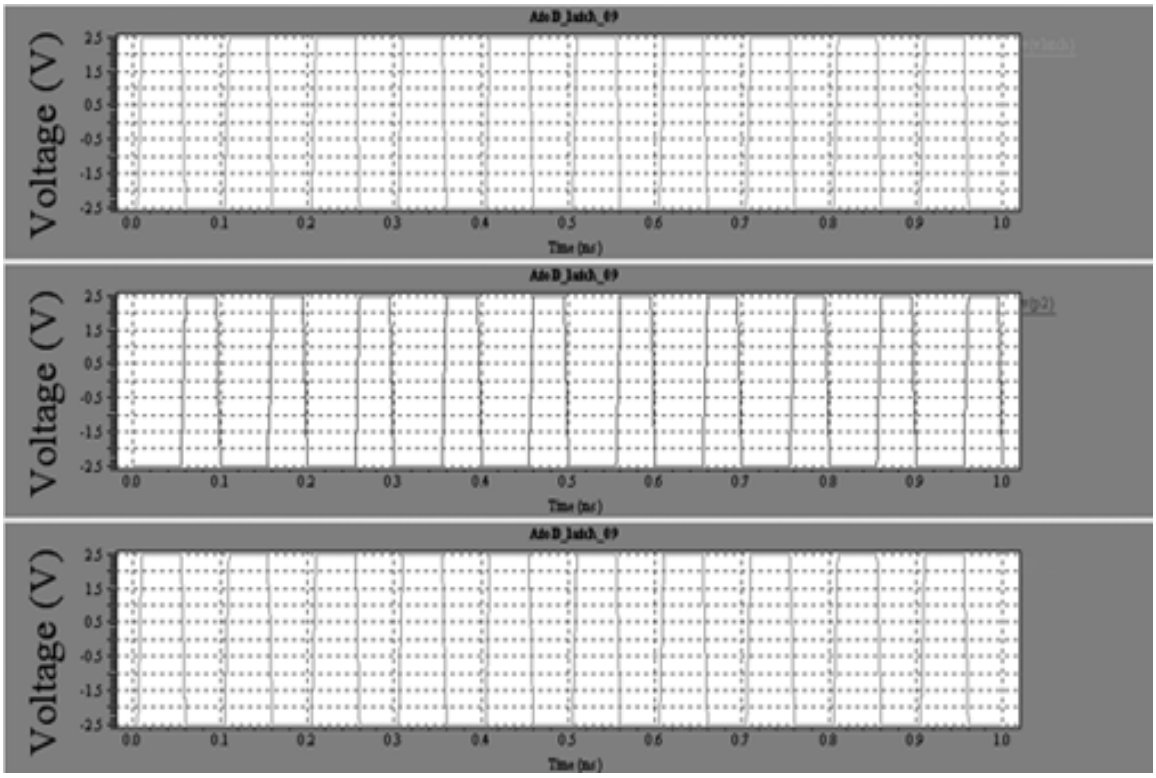

Figure 3.11: Pulses Used to Drive the ΣΔM

As illustrated, pulses p1 and p2 are completely out of phase with each other. These signals are used to drive the switches of the switched capacitor filter. Pulse vlatch is in phase with p2 and is used as the latching signal for the latched comparator.

A simple transient analysis was used to simulate the output of the circuit. The simulation commands are shown below:

.tran/op 1e-3 .001 method=bdf

.print tran v(vout+, vout-) v(vin+, vin-)

The first statement instructs the simulation tool to perform a transient analysis from 0ms to 3ms. The second command displays the results of the simulation on W-Edit. As shown, the output of this circuit is taken at the non-inverting output of the circuit with respect to the inverting output. Figure 3.12 illustrates the simulation results. As illustrated, a DC voltage was applied to the inputs of the modulator.

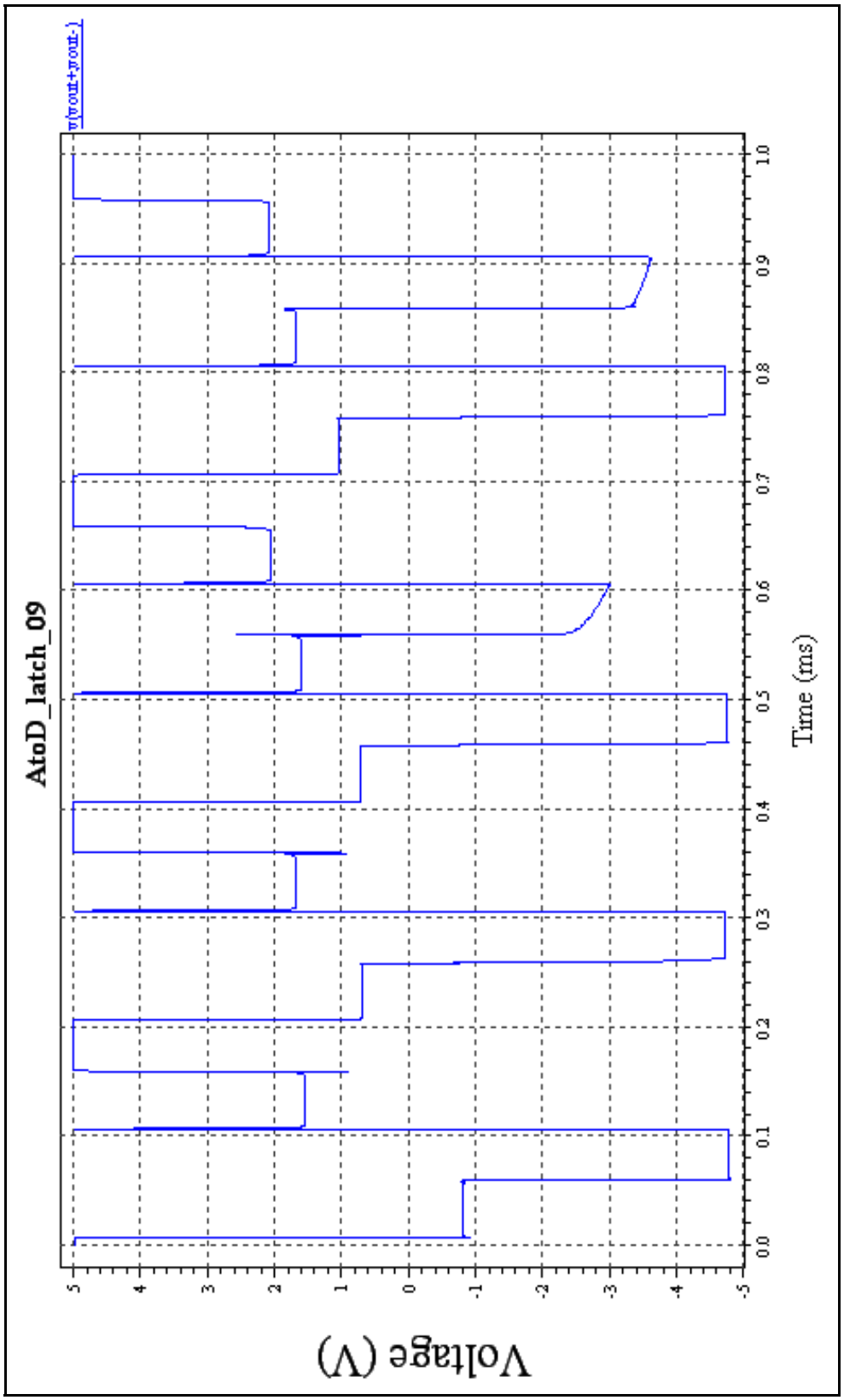

Figure 3.12: ΣΔM Simulation Results Using DC Input

The simulation results show that the modulator was able to produce several pulses that are nearly identical. As one would expect, a continuous analog input does indeed produce a constant, discrete output. In addition, some distortion which was possibly a result of noise effects or an offset is clearly present. These results seem to indicate that the modulator operates as intended. However, additional simulations reveal that the circuit is only sTable between a DC input of -1.25VDC and +1.5VDC.

The transfer characteristics of the modulator were measured by counting the ratio of high to low pulses for a 0ms to 1ms simulation. A high pulse is defined as anywhere where the output is above zero. Likewise a low pulse is anywhere the output was observed below zero. For each simulation, the input voltage applied to vin+ was varied from -2.5VDC to +2.5VDC. This "pulse counting" technique is illustrated in Figure 3.13.

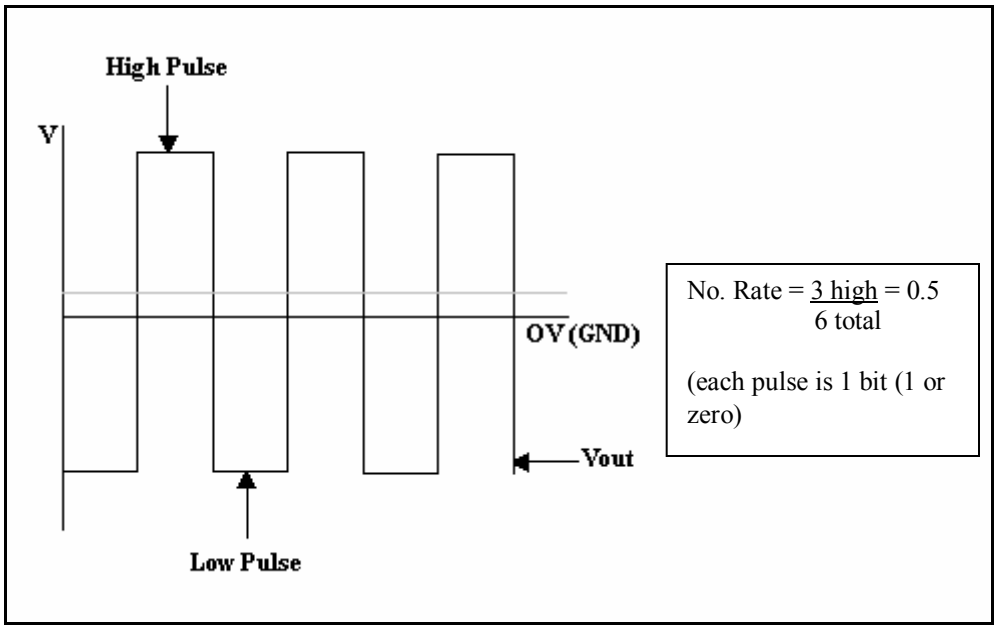

Figure 3.13: Pulse Counting Technique

The modulator transfer characteristics are shown in Figure 3.14.

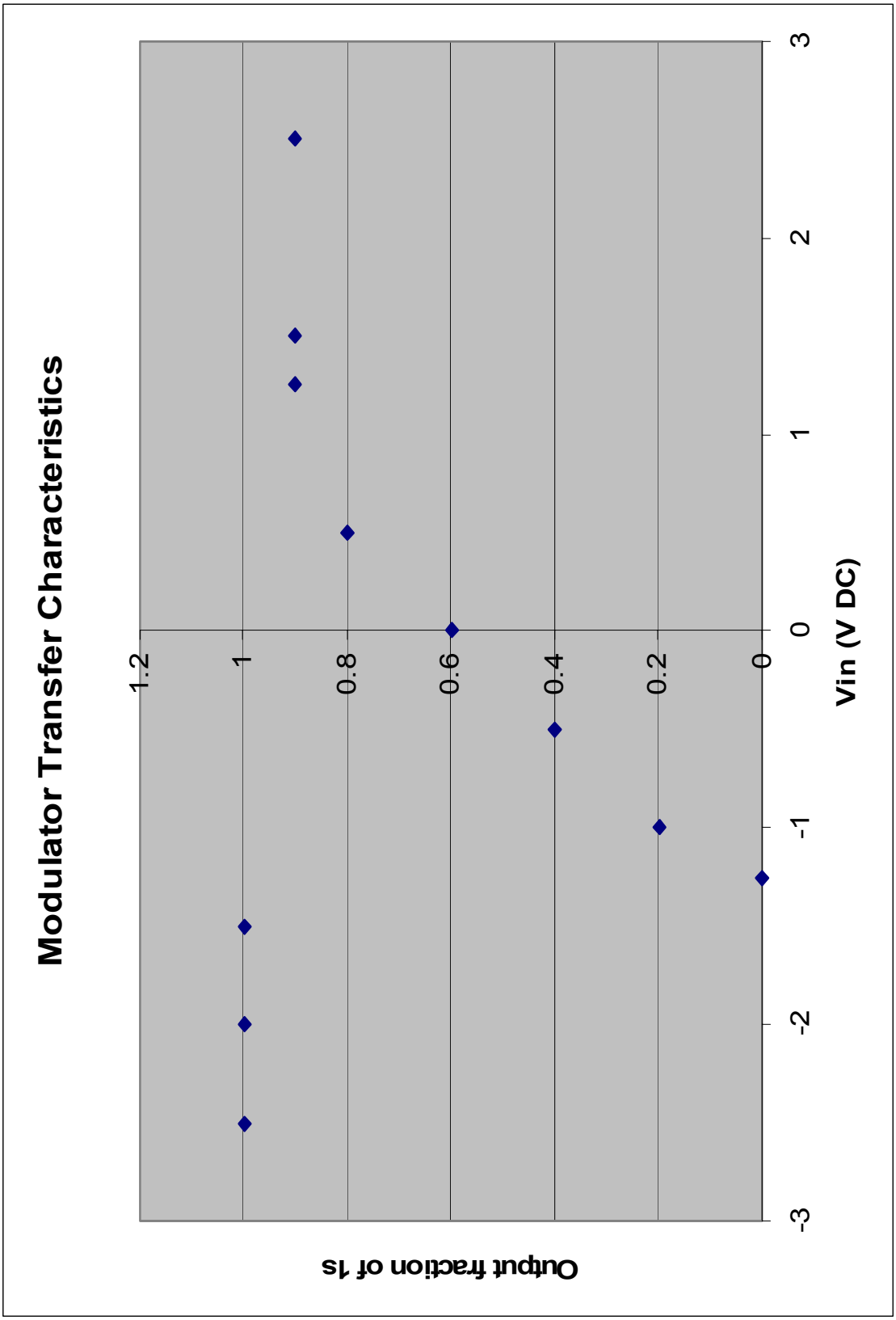

Figure 3.14: ΔΣM Transfer Characteristics

In each case, the circuit was able to nearly achieve a one-to-one ratio for the number of high to low pulses. However, the converter only operates (linearly) between -1.5V and +1.25V. In addition, the entire circuit consumed approximately 67.2mW of power.

3.6 Design Submission

Each of the designs that are described in this report was fabricated using an AMI 0.5um process. The first design (analog_09) which is shown in Figure 3.15, was submitted under a MOSIS Educational Program (MEP) classroom account. This account allows that five parts (IC's) be fabricated and bonded to a DIP40 package.

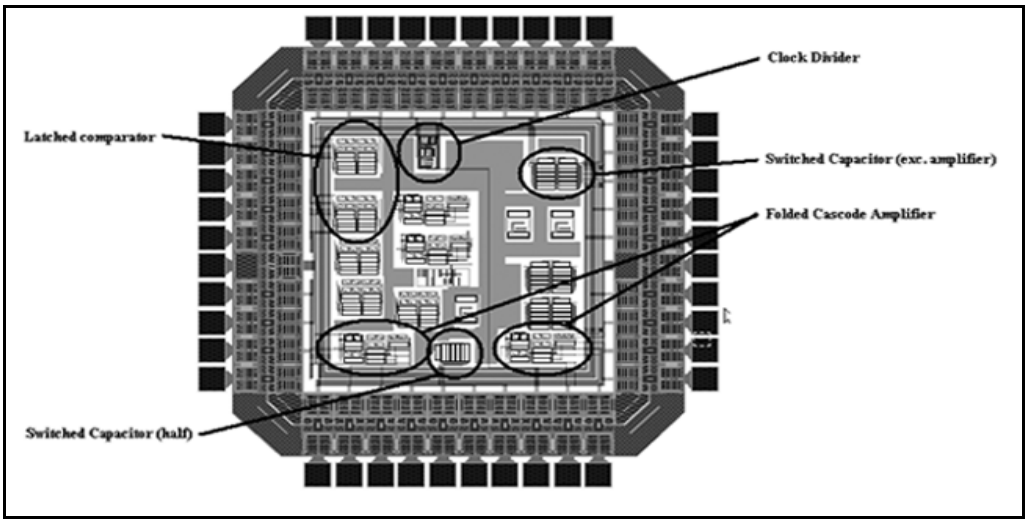

Figure 3.15: Completed Design- Analog_09

As Figure 3.15 illustrates, analog_09 contains four unique parts. Two identical versions of the folded cascode amplifier and latched comparator were placed on the chip. In the event that one design was flawed as a result of fabrication error, there will always be a duplicate part to test.

Next, the capacitors and switches of the switched capacitor filter were placed on the chip. It is important to note that this version of the filter utilizes large transistors. The final part shown in the design is a clock divider. The clock divider or clock splitter separates a square wave into two waves that are completely out of phase with one another. This circuit may later be used to drive the switched capacitor filter, which requires two unique clock pulses.

The remaining space on the chip was filled with unwired duplicates of each part. In addition, any empty space on the chip was filled with poly to meet the minimum poly requirements of the process.

The second design (analog_10), which is illustrated in Figure 3.16, was submitted under a MEP research account. This account requires that a minimum of forty-five parts be fabricated. However, to reduce costs, only five parts were bonded to a DIP40 package.

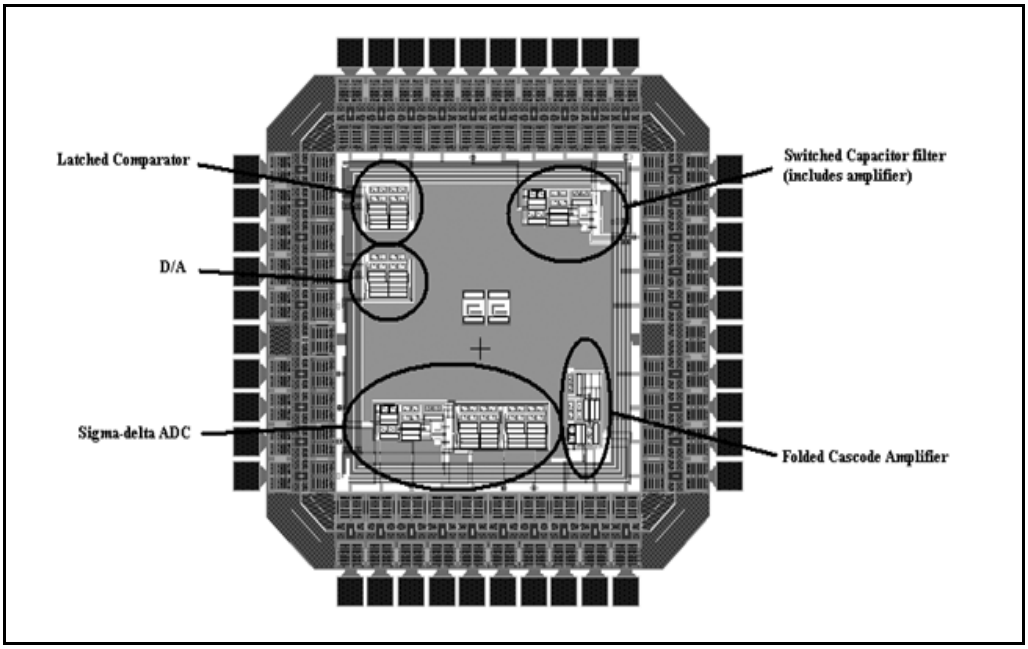

Figure 3.16: Completed Design – Analog_10

As shown, this design contains a total of five unique parts. Of greatest importance is the inclusion of a complete ΔΣ modulator. This circuit contains the latched

comparator, switched capacitor filter (uses the folded-cascode amplifier and small filter switches) and D/A.

Next, a folded-cascode amplifier and latched comparator were placed on the chip. Both of these parts are identical to the parts submitted on analog_09. In addition, an independently wired D/A and switched capacitor filter were placed and routed. The switched capacitor filter utilizes the smaller, updated switched and the folded-cascode amplifier.

4. SUMMARY AND CONCLUSIONS

The design and simulation of a first-order, sigma-delta modulator (ΣΔM) has been proposed and discussed in this Thesis. This type of modulator is recognized for its noise-shaping abilities and consists of two basic parts; an integrator and a quantizer. The integrator is used to sample an analog input and convert it to a low resolution digital output. The quantizer converts the low resolution signal from the integrator to a high resolution digital output.

The modulator was created by scaling some preexisting designs from an older process and combining them with new circuits to form the completed circuit. The process of scaling designs to a new minimum feature size required that several key changes be made to the circuit design tools. Some of these changes were simple such as modifying the circuit design rules or adding new layers to the layout tool. Other modifications, such as updating the extraction file for the layout tool, proved to be more difficult.

After the necessary changes had been made to the circuit design tools, the updated tools were used to scale an existing design of the folded-cascode amplifier for later use in the modulator. The simulation results show that the updated design of the folded-cascode amplifier was able to achieve a higher gain and larger gain bandwidth when simulated with the 0.5um parameters. The 1.6um simulation of the amplifier was able achieve a gain of 50dB with a unity gain bandwidth of approximately 700KHz. The 0.5um simulation of the circuit was able to achieve a gain of 60.55dB and a unity gain bandwidth of approximately 10MHz. A comparison of these results shows that the 0.5um process was able to realize an increase of 10.55 dB. In addition, the unity gain bandwidth of the 0.5um simulation increased by 300Hz.

Moreover, the updated tools were used to create several new designs for the modulator. New designs were created using a "standard cell" approach. This approach calls for the implementation of pre-designed and pre-tested sets of transistors. The advantages of this approach include:

- *Quick turn around.*

- *Simplified schematic-entry*.
- *Simplified layout*.
- *Faster verification times.*

The disadvantages of using this approach include:

- *Wasted wafer space.*
- *Slew rate and switching time reduction*.
- *Low output swing*.

The "standard cell" approach was used for the design of a switched capacitor filter, latched comparator, D/A and the completed ΣΔM. The output of the switched capacitor filter illustrates that the circuit operates as intended. Moreover, the filter output was affected very little by the process transition. In each case, the cutoff frequency of the filter remained unchanged, however, the offset of the filter used in the 0.5um simulations increased by 0.03V.

During its initial stages of development, the latched comparator was implemented by attaching slew-limiting circuitry to the output of the folded-cascode amplifier. Unfortunately, as the project progressed, it became evident that this circuit was unable satisfy the required specifications for the modulator. Consequently, a new circuit was designed and simulated that was able to meet the slew rate and gain requirements for analog-to-digital conversion. The simulation of the latched comparator revealed that the circuit operated as intended.

The D/A was created by modifying the schematic of the latched comparator. The latch signal was removed from the original circuit and an additional bias was used to control the current through the circuit feedback loop. It was anticipated that limiting the amount of feedback would have a scaling effect on the output of the D/A. Unfortunately, as shown in the simulations, altering the bias voltage did not have the desired effect on the output of the circuit.

Finally, the designs of the switched capacitor filter (which included the folded-cascode amplifier), latched comparator and D/A were combined to form a complete

modulator. Initially, the modulator was simulated by applying a sine wave to the inputs of the circuit. This type of simulation appeared to surpass the capabilities of the circuit design tools so as a result, the circuit was simulated using a DC input. Simulations of the modulator illustrate that the circuit is able to achieve a modulated, digital output of the DC input. However, the output of the ΣΔM is limited to a narrow range of operations between -1.5VDC and +1.25V DC.

5. RECOMMENDATIONS FOR FUTURE WORK

In general, most of the circuits that are included in this Thesis operated as intended. In some cases, revised designs such as the folded-cascode amplifier were able to achieve higher gain and greater stability when simulated using the updated process parameters. However, there is always room for improvement as suggested by the output of the D/A and the completed modulator.

At the conclusion of this experiment, it became evident that the size of this circuit surpassed the capability of the design tools. T-Spice^{TM} was able to effectively simulate the individual parts of the design, but it was only able to provide a rudimentary idea of the output of the completed ΔΣM. Initially, the ΔΣM was simulated by driving the non-inverting input of the circuit with a sine wave and grounding the inverting input. It was anticipated that by using this approach, the circuit would yield a quantized version of the sine wave. However, due to circuit complexity, the simulation tool was not able to produce any kind a recognizable output. Consequently, the design was re-simulated by driving the circuit with a DC signal.

It is also interesting to note that different versions of the simulation tool produced strikingly dissimilar results. For example, an amplifier that may have achieved 60db of gain in an old simulation engine may only yield 40db of gain using a later simulation engine. Consequently it is recommended that in the future, the following changes be made to the simulation approach:

- *Use different design/simulation tools*. As previously explained, it has been found that the circuit design tools are not able to effectively simulate a circuit of this complexity. Therefore, I suggest that the circuit be simulated with another tool that is able to produce consistent results.
- *Re-simulate the ΔΣM using different constraints.* That is to say, that design should be re-simulated by driving the circuit with a sinusoidal signal. While the DC analysis seems to indicate that the ΔΣM is working properly, it would be advisable to confirm this using another type of simulation.

Next, the simulations of the D/A illustrate that while this part is functional, it does not appear to be very effective. The bias voltage does not appear to have the desired "scaling" effect on the output of the circuit. Consequently, I suggest that the existing D/A design either be revised or replaced. The new design should include a D/A that is able to produce the desired effect and is able to switch very quickly.

After that, as the simulation results illustrate, the modulator has a very narrow range of stability. It was only after some fine tuning of *VREF+* and *VREF-* that the circuit was able to produce a steady, sTable output. Some of this problem can be attributed to the low current requirements of the design. One of the consequences of a low power, low current design is that the circuit is unable to achieve a very wide output swing. In the future, the aspect ratios of the circuit should be adjusted to obtain the widest swing possible.

After the modulator has been fine-tuned, additional stages could be added to produce more resolution. This experiment could be performed quickly and easily by copying and pasting several identical stages of the modulator.

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